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Sub-Band Digital Predistortion for Noncontiguous Carriers: Implementation and Testing
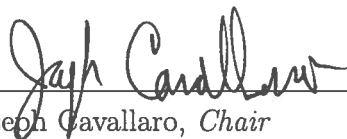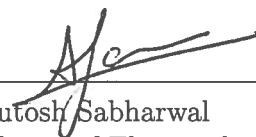
by

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ABSTRACT

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To facilitate increasing data-rate demands and spectrum scarcity, non-contiguous transmission schemes are becoming more popular. However the non-contiguous carriers of such schemes intermodulate due to the non-linear nature of power amplifiers (PAs). This may cause emissions which interfere with nearby channels or with one's own receiver in a frequency division duplexing transceiver. We implement a low-complexity, sub-band, block-adaptive, digital predistortion (DPD) solution that corrects the distortion in a real PA. Using WARPLab we correct up to ninth-order nonlinearities, and using a real-time FPGA design we correct up to third-order nonlinearities. This is done by targeting the most problematic spurious distortion components at the PA output and performing least mean squares training to adapt an inverse spur to inject. This sub-band method allows for reduced processing complexity over other full-band predistortion solutions. Using these techniques, we are able to suppress spurious emissions in WARP by over 20 dB.

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INTRODUCTION

1.1 Motivation and Problem Statement

There has been tremendous growth in wireless communications over the last twenty years. To illustrate this, consider cellular telephones. The number of cellphones in use at any time has been growing continuously since their invention. The growth has been so strong, that it is estimated that there will be over 2 billion smart phones in use on the planet by the end of 2016 [1]. Moreover, many of these wireless devices are demanding faster data rates for services such as streaming HD video and music, email, social networking, and general internet usage. In fact, a significant portion of people use their mobile devices as their primary terminal for internet activities [2]. This increase in the number of users and activity is undeniably a challenge for nearly all facets of wireless design.

We have seen average download and upload speeds increase over the years to accommodate the increases in demand. Many of the speed increases are the result of increasing bandwidths (BWs). However, when the number of wireless users increases and the average bandwidth per user also increases, spectrum can quickly become scarce. It is necessary to efficiently use available spectrum. Cognitive radio (CR) is

one proposed way to go about this that has received attention. With CR a wireless user may use spectrum that is allocated to another licensed, primary user when that primary user is not present. By doing this, spectrum congestion in some of the more active bands can be alleviated by offloading to other less congested bands [3] [4]. For this to be feasible, the secondary users' transceivers must be designed to be what is referred to as "frequency agile."

This concept is not exclusive to CR. Even in a system that operates entirely in licensed bands, whenever channels of spectrum are busy, it may be necessary to dynamically use available channels and be more frequency agile such as in these CR systems. To maintain desired data rates, it may even be necessary to use multiple channels simultaneously. We see this in 4G systems and other standards already today. In LTE-Advanced, multiple channels are used simultaneously through carrier aggregation (CA) [5], and in IEEE 802.22 the aggregation of several carriers is done through what is referred to as "channel bonding" [6]. This is also a strong motivation for the successor to 4G technologies which are still being developed and which are referred to as 5G. To achieve data rates for 5G which are on the order of 1 Gbps, major points of change over 4G include better spectral efficiency and increased bandwidth. Moreover, lower cost and better energy efficiency are also desired. However, this non-contiguous type of transmission is considered to be a major challenge going forward for both 5G [7] [8] and cognitive radio [9].

In this thesis, we consider non-contiguous transmission in the context of carrier aggregation for LTE-Advanced though the methods could generalize to other non-contiguous transmissions. There are three different categories of CA. Firstly, there is intra-band, contiguous. Here, as the name suggests, all the component carriers are adjacent and within the same LTE band. Secondly, there is intra-band, non-contiguous which is in the same band but at least two of the carriers are separated

Intra-band, Contiguous:

Band A

f

Intra-band, Non-contiguous:

Band A

f

Inter-band, Non-contiguous:

Band A   Band B

f
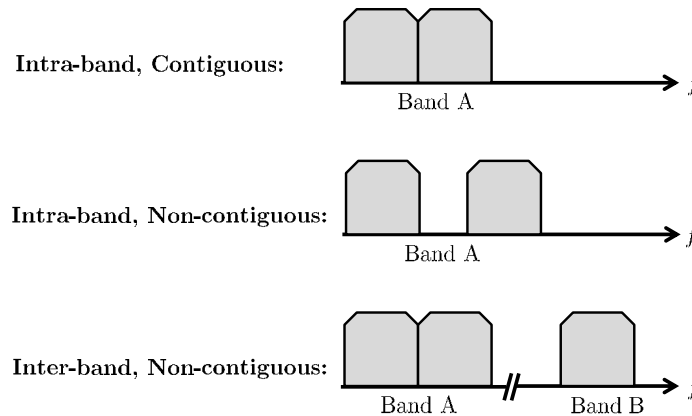
Figure 1.1: Types of Carrier Aggregation

by some bandwidth. Finally, there is inter-band, non-contiguous where multiple LTE bands are used simultaneously. This is illustrated in Figure 1.1.

Release 12 of the LTE-Advanced specifications allows for up to 5 carriers which corresponds with up to 100 MHz bandwidth [5]. The latest Qualcomm [10] and Samsung [11] system on chips (SOC) support this for up to three carriers each with a 20 MHz bandwidth. Networks have started to role out support for carrier aggregation as well. For example, the Sprint LTE Plus network currently supports carrier aggregation for two carriers [12].

Although support is growing, there is still a major problem with using some forms of carrier aggregation. Non-contiguous transmissions do not behave well with power amplifiers. This is due to the nonlinear behaviour seen in the PAs especially at high gains. In particular, the carriers intermodulate to create intermodulation distortion (IMD) spurious emissions or "spurs." These spurs could be interfering with neighboring channels or could interfere with ones own receiver in a frequency division duplexing (FDD) transceiver [13]. Moreover, this is even more notable in more economical devices like mobile, LTE-Advanced user equipment (UE) where cheaper, less linear PAs may be used. To add to the problem, modern wireless communication systems typically use multicarrier type modulations with very large peak-to-average

power ratio (PAPR) like OFDM, OFDMA, and SC-FDMA. So when considering the inherent nonlinearities of the PA, the PAPR of signals, the upcoming non-contiguous transmission schemes, and the high power-efficiency restraints for mobile devices, it is apparent that controlling the unwanted emissions is a significant challenge. This problem will be only become more present as networks and cellular devices continue to upgrade to better support carrier aggregation with the current standards and future 5G standards.

For mobile devices, being energy efficient is a fundamental design goal, and since the power amplifier is one of the most demanding components in terms of energy for mobile transmitters, we must consider its efficiency. For non-contiguous schemes, it has been shown that it is more power efficient to combine the carriers before the PA [14]. However, this configuration is what leads to severe IMD spurs. Also, PAs are most power efficient when operating at higher gains. This is well known and directly apparent in data sheets. For example, a common LTE PA such as the Anadigics ALT5020 has an efficiency of 38% when operating at a high power but is only 13% efficient when the power is 20 dBm less [15]. However, operating in this high-gain saturation region is where the PA is also most nonlinear and hence has the most distortion.

Although PAs are most power efficient in saturation, it is necessary to avoid the distortions, so it is common to back off on their transmit power to avoid the distortions. This is referred to as maximum power reduction (MPR) [16]. Although this reduces the relative strength of distortions to be within allowed tolerances, it forces the PA to operate in a less efficient region. This is not desirable especially in mobile devices. Moreover, by reducing the peak power the network coverage is also reduced. Therefore there is a need for a low-complexity method to suppress the spurious emissions so that the device can operate in saturation.

One possible approach that has received extensive research attention is transmitter linearization through what is known as digital predistortion (DPD) [17]. This can be seen as early as 1981 with an early DPD patent [18]. In this patent, there is feedback from the transmitter that is used to adaptively select a predistorter. Bell labs also shows some similar work on an adaptive method focusing on transmitter linearization [19] that only works for memoryless nonlinearities.

Research on the topic has continued steadily with various architectures being used for linearization. However, most research focuses on linearization for single carrier schemes which is not helpful for non-contiguous CA. There is also DPD research being done in industry. Its importance is noted for example by Keysight Technologies. In their work, they consider CA for LTE-Advanced. However, they only consider contiguous cases [20]. This and many other DPD methods seek to linearize the full composite carrier which we will refer to as "full-band DPD." These schemes are also often targeted at base-stations and may be too computationally complex for mobile transmitters.

There has been a few recent works that consider multi-band transmitters with a single PA. However, it is assumed that the spacing between the component carriers is large so that spurious emissions are filtered out by the transmit radio-frequency (RF) filter. Hence only the main carrier is linearized [21] [22]. In [23] and [24], it was assumed that a the PA had no change in response depending on frequency. They then model the memoryless PA parameters offline to cancel the nonlinearities. This work is not adaptive and flexible enough to be used in real systems.

Various DPD implementations have been considered. One possibility considered recently is graphics processing units (GPU) [25] [26]. These works do consider non-contiguous scenarios. However, they are full-band and therefore can encounter similar problems with respect to complexity like other full band techniques. Also, these works

rely on offline training. Moreover, GPU implementations tend to be higher power consumption and are likely not to be the most energy-efficient implementation for a mobile device.

Most forms of DPD are too complex for mobile devices and do not consider the non-contiguous case. In work proposed and simulated in [27], this problem was addressed. The DPD used in this paper targets IMD spurs to selectively suppress only spurs in violation of emission limits. By targeting only the ones that are in violation, computational complexity can be significantly reduced. However, this work has been largely theoretical with some simulations. It is the principle goal of this thesis to fully test this algorithm in the context of an actual power amplifier. By doing so, we hope to move this work from the theoretical domain into the practical domain.

1.2 Background

The problem presented previously in the introduction of this thesis and its solution discussed throughout the thesis is complicated and involves theory from many subjects. These include and are not limited to solid state physics, nonlinear systems, computer architecture, etc. Selected topics are chosen for discussion here to help provide relevant background material to the reader.

1.2.1 Peak-to-Average Power Ratio

Peak-to-average power ratio (PAPR) is defined in Equation 1.1 for any signal x.

$$\text{PAPR}_{dB} = 10 \ \log_{10} \frac{\max\left(|x|\right)^2}{x_{\text{RMS}}^2} \tag{1.1}$$

Non constant envelope signals lead to poor PAPR. This is especially true for orthogonal frequency-division multiplexing (OFDM) which is used for LTE downlink

signals. A high PAPR can be unacceptable for a few reasons. Firstly, regulatory constraints often limit the maximum power. For signals with a high PAPR, this leads to the average power of the signal being lower which can reduce range. Also, if the signal is on average in the linear region of power amplifier operation, then there will likely be peaks that are operating in the saturation region which leads to stronger spectral regrowth and intermodulation emissions [28].

Although the PAPR for single carrier frequency-division multiple access (SC-FDMA) which is used for the uplink in LTE is lower than OFDM [29], it is still large as shown below and leads to significant spurs as shown throughout this thesis. Using Equation 1.1, we numerically calculate the value for a QPSK, OFDM LTE downlink signal with two 1.4 MHz carriers spaced by 6.7 MHz to be 11.9 dB. This is a typical value for OFDM systems and is problematic. Using similar signal parameters but using SC-FDMA as in an LTE uplink signal, we calculate the PAPR to be 9.2 dB. So although the PAPR for SC-FDMA is in this case better than OFDM by 2.7 dB, it is still significant and will contribute to IMD distortion.

1.2.2 Power Amplifiers

An RF power amplifier is an essential component in all wireless devices. To illustrate this, consider the Maxim 2828 WiFi transceiver which is used in the WARP software defined radio (SDR) platform. The maximum output power for a continuous wave signal is only -2 dBm [30] or about half a miliwatt.

Using the Friis Free Space Equation shown as Equation 1.2, we can calculate a hypothetical received power for various scenarios. In this equation, P_r is the received power, λ is the wavelength, d is the distance of propagation, P_T is the transmit power,

G_R is the receive antenna gain, and G_T is the transmit antenna gain.

$$P_R = \frac{\lambda^2}{(4\pi d)^2} P_T G_r \tag{1.2}$$

Assuming no antenna gain, 2.4 GHz frequency, a distance of 50 meters, and the previous -2 dBm transmit power, the equation becomes

$$\begin{aligned}
P_R &= \frac{(0.125m)^2}{(4\pi 50m)^2} 0.5 \\
&= \frac{0.015625m^2}{394784} 0.5 \ mW \\
&= 1.97 \times 10^{-8} \ mW \\
&= -77 \ dBm
\end{aligned}$$

In this scenario, the received signal is difficult to detect. Detection becomes nearly impossible as interference, path loss, and other factors make this worse. Power amplifiers bridge the gap and make it possible to transmit longer distances.

Power amplifiers were historically made with vacuum tubes. Tubes amps may still be chosen for some high power basestations, but typical power amplifiers are made with transistors such as metal-oxide-semiconductor field-effect transistors (MOSFETs) or bipolar junction transistors (BJTs). For many high frequency applications, BJTs are chosen [31]. For example, the power amplifier for the WARPv3 board that is considered throughout the thesis is a heterojunction-bipolar-transistor device fabricated with InGaP GaAs technology. There are multiple general modes of operation for BJTs. From studying BJT operation modes and the voltage current relationships, it is apparent that the devices are largely nonlinear.

Moreover, there are memory effects in a power amplifier. The output at any instance depends partially on previous inputs. Memory effects are attributed to

thermal and electrical effects. The electrical memory effects are the most prominent and are mostly attributed to a non-constant frequency response of the PA around the carrier frequency [32].

1.2.2.1 Models

Understanding the nonlinearities in a power amplifier is essential to be able to attempt any form of linearization. To do that, we must first consider various models. When attempting to model a power amplifier, the most intuitive first attempt may be to do a polynomial fit via a Taylor Series. However this does not consider the memory effects of the device. To consider memory effects, we go to a Volterra series. This is one of the most general forms for modeling a nonlinear system. In essence, it is simply a Taylor series with memory and has the form of Equation 1.3.

$$y(t) = \mathbf{H}_1[x(t)] + \mathbf{H}_2[x(t)] \cdots \mathbf{H}_n[x(t)] \cdots \tag{1.3}$$

In this equation, $\mathbf{H}_n$ is the Volterra operator given by Equation 1.4 where the order n represents the memory order [33].

$$\mathbf{H}_n[x(t)] = \int_{-\inf}^{\inf} \cdots \int_{-\inf}^{\inf} h_n(\tau_1, \ldots, \tau_n) x(t - \tau_1) \cdots x(t - \tau_n) d\tau_1 \cdots d\tau_n \tag{1.4}$$

Although the Volterra series is a powerful tool, it can be difficult to extract parameters to generate a model. Wiener recognized this and made assumptions to simplify the equation. He developed a new model that separated the memory components from the nonlinear components. This is seen as a linear time invariant (LTI) system in series with a nonlinear system. By separating the nonlinear system and the memory system, analysis can become easier. This has been used to model power amplifiers
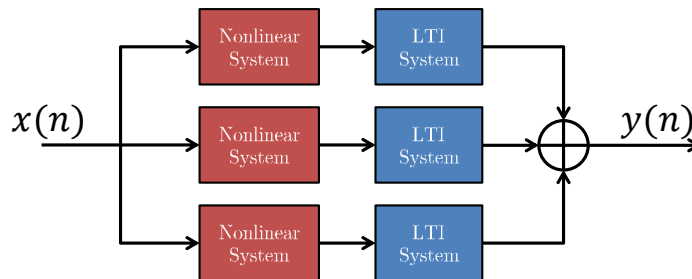
Figure 1.2: Structure of a Parallel Hammerstein nonlinear model

and has been used for some DPD schemes.

A Hammerstein model is similar to a Wiener model in that there is an nonlinear and LTI element in series. However, instead of a LTI element followed by an nonlinear element, the nonlinear element is first in the model.

The final model that is commonly used combines the Wiener and Hammerstein into one system called a Wiener-Hammerstein model. It consists of an LTI element, followed by a nonlinear element, followed by another LTI element. For any of these systems, it is possible to consider a parallel structure to account for multiple nonlinear basis functions as we will do later in this thesis with the Parallel Hammerstein structure. We illustrate this in Figure 1.2. Here, the term "basis function" is used as it is throughout the DPD literature. In a more rigorous and strict mathematical sense, the term basis implies that the a linear combination must be able to span some space. Here, although we do not show it in detail, the basis functions will span a spurious emission's contents based off the PA model.

1.3   Contribution

Although DPD is not a new concept, most of the work has concentrated on single carriers. The work that has been done considering non-contiguous transmissions has been largely theoretical with testing done using simulations based on power amplifier

models. In this thesis, we evaluate one such algorithm using real hardware. We present a WARPLab implementations for IM3 spur suppression that accounts for up to ninth-order nonlinearities and present a field-programmable gate array (FPGA) implementation for a 3rd order IM3 spur suppression.

In [34], we presented the first results of this and a block-based method was introduced for real-time scenarios. The third order nonlinearities are also suppressed using the WARPLab platform for offline training and in an FPGA design. We expand on that work to include higher order nonlinearities, and we also consider larger bandwidths in the WARPLab platform.

In spirit, this method of DPD is similar to a full-duplex scenario. In full-duplex, feedback from the receiver is used to subtract out ones own transmissions from receiver. This has been researched and even implemented using the WARPLab platform [35]. However, to best of the author's knowledge, an FPGA implementation has not been done for such a system. With this context, it is clear that the FPGA development work is especially novel.

1.4 Thesis Overview

The thesis is organized as follows. In Chapter 2, an overview of the algorithm is presented. In Chapter 3, the experimental results obtained from WARPLab are presented. In Chapter 4, a discussion of the FPGA architecture along with experimental results from the FPGA design are presented. In Chapter 5 we conclude the thesis and propose future work.

ALGORITHM OVERVIEW

The algorithm has been developed in the literature over the course of multiple papers. These include [27] and [34]. The majority of the content in this chapter reflects that work and a journal article currently under review for *Transactions on Microwave Theory and Techniques*. This work is primarily developed by Mahmoud Abdelaziz at the Tampere University of Technology in Finland.

2.1   Intermodulation

Whenever two or more signals of different frequencies are the input to a nonlinear system, intermodulation may occur. The system will have an output that consists of sum and differences of the input frequencies multiplied by integers as given in Equation 2.1 where $n, m \in \mathbb{Z}$.

$$f_{IM} = nf_1 \pm mf_2 \tag{2.1}$$

The order p is given by the sum of the absolute value of integer coefficients n and m. So for any arbitrary tones f_1 and f_2 the p_{th} intermodulation terms exist at frequencies

corresponding to these sums. For example, the IM3 tones exist at $2f_1 \pm f_2$, and $2f_2 \pm f_1$ [36].

2.2 Spurious Component Modeling

We start by assuming that there are two signals that are represented at baseband by $x_1(n)$ and $x_2(n)$. Let them be each shifted by some intermediate frequency, f_{IF}, so that the spacing between them becomes $2f_{IF}$. The composite baseband input to the PA becomes as shown in Equation 2.2.

$$x(n) = x_1(n)e^{j2\pi \frac{f_{IF}}{f_s}n} + x_2(n)e^{-j2\pi \frac{f_{IF}}{f_s}n} \tag{2.2}$$

We use a Parallel Hammerstein PA model for the following. It is a widely used choice for modeling power amplifiers and has proven to be an accurate model [37]. Consider an order P model with monomial nonlinearities. This is given in Equation 2.3.

$$y(n) = \sum_{\substack{p=1 \\ p \text{ odd}}}^{P} f_{p,n} \star |x(n)|^{p-1} x(n) \tag{2.3}$$

In Equation 2.3, $f_{p,n}$ is the FIR branch filter impulse response of order p, and $\star$ is the convolution operator. We illustrate this is the block diagram shown in Figure 2.1. This output of this system is illustrated for two carriers with up to the fifth nonlinearity order considered in Figure 2.2. In this figure we see that lower order spurs such as IM3 spurs are comprised of distortion from nonlinearity terms equal to and greater than its own order.

As started earlier, there will be intermodulation spurs at multiples of sums and differences of the input frequencies. Because the components are equally spaced
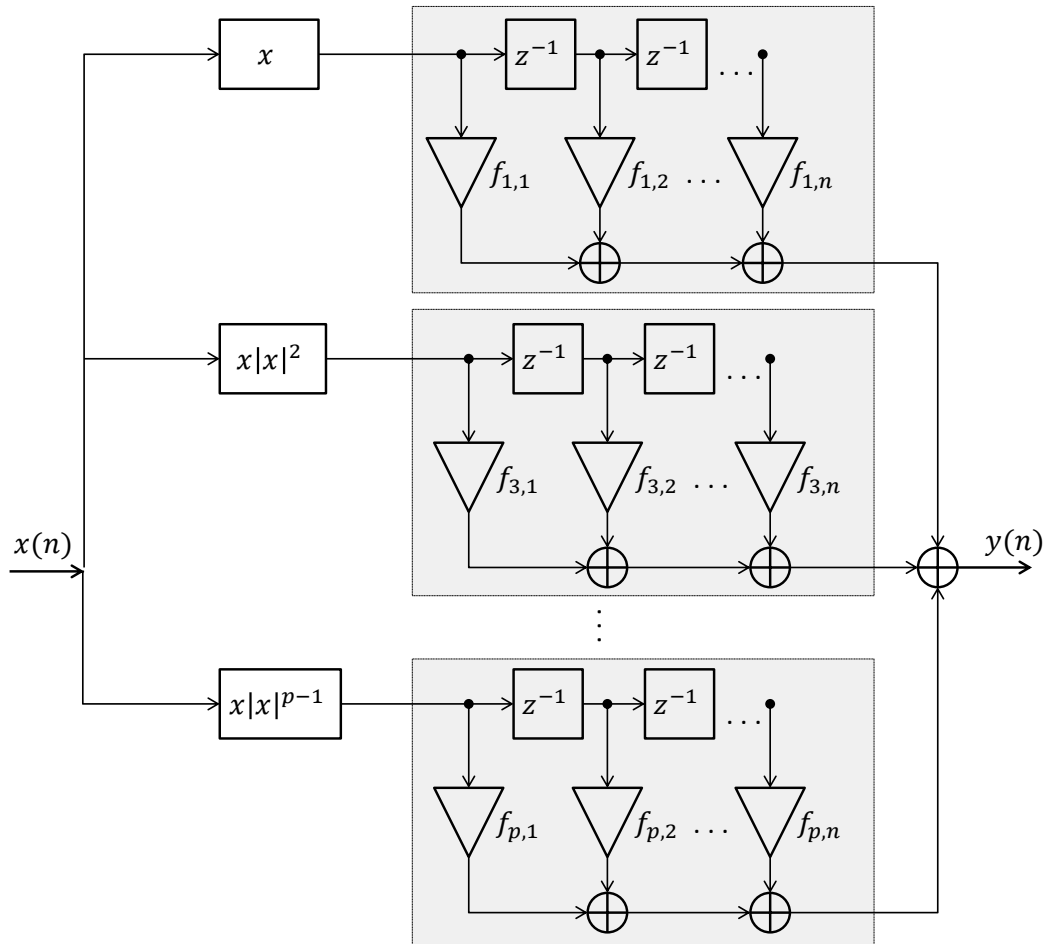
Figure 2.1: Block Diagram of Parallel Hamerstein PA Model
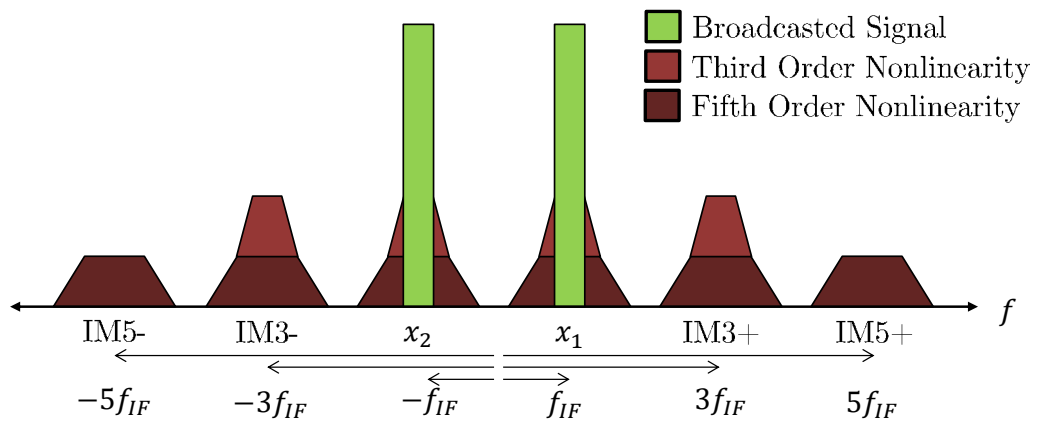

Figure 2.2: Intermodulation Spurs

around baseband, Equation 2.1 simplifies giving us Equation 2.4. This places the $IM3$ spurs at $\pm 3 f_{IF}$, the $IM5$ spurs at $\pm 5 f_{IF}$, etc.

$$f_{IMD_p} = (n \pm m) f_{IF} \tag{2.4}$$

Suppose equation 2.2 is substituted into 2.3 with $P = 3$. If we were to expand out and collect all terms that contain $e^{2\pi j \frac{3 f_{IF}}{f_s}}$, then we would find a term like Equation 2.5. This equation is the third-order, nonlinear basis function that exists at a frequency of $3 f_{IF}$ which is the IM3+ spurious emission written at baseband.

$$u_{3+,3}(n) = x_2^*(n) x_1^2(n) \tag{2.5}$$

If we were to repeat this but to increase P to include higher order nonlinearities, we would find more terms that contribute to this spur caused by these higher order nonlinearities. These are included below as Equations 2.6 – 2.8 where we consider up to a nonlinearity order of nine. Each of these are written at baseband. We use notation that defines nonlinear basis functions $u_{IMD,p}(n)$ with the first subscript denoting the spur that it corresponds to and the second denoting the nonlinearity order that created it. The complex conjugate is denoted by $*$. The basis functions can also be obtained for the negative IM3 spur (IM3-) similarly. They simplify to be the same as the IM3+ basis functions except we substitute x_1 for x_2 and vice versa.

$$u_{3+,5}(n) = u_{3+,3}(n) \times \left(2 \left| x_1(n) \right|^2 + 3 \left| x_2(n) \right|^2 \right) \tag{2.6}$$

$$u_{3+,7}(n) = u_{3+,3}(n) \times \left(3 \left| x_1(n) \right|^4 + 6 \left| x_2(n) \right|^4 + 12 \left| x_1(n) \right|^2 \left| x_2(n) \right|^2 \right) \tag{2.7}$$

$$u_{3+,9}(n) = u_{3+,3}(n) \times \left(5 \left| x_1(n) \right|^8 + 15 \left| x_2(n) \right|^8 + 60 \left| x_1(n) \right|^6 \left| x_2(n) \right|^2 \right.$$
$$\left. + 100 \left| x_1(n) \right|^2 \left| x_2(n) \right|^6 + 150 \left| x_1(n) \right|^4 \left| x_2(n) \right|^4 \right) \tag{2.8}$$

With this notation, we revisit the substitution of Equation 2.2 into Equation 2.3 again considering the $IM3+$ spur. The output at $3f_{IF}$ can now be written as as Equation 2.9. This represents the contribution of each nonlinearity to the IM3+ spurious emission. In this equation, f is the FIR filter that models the memory associated with the term and $u_{3+,p}$ are the corresponding p^{th} order nonlinear basis functions.

$$y_{IM3\pm}(n) = \sum_{\substack{p=3 \\ p \text{ odd}}}^{P} f_{3\pm p,n} \star u_{3\pm,p}(n) \tag{2.9}$$

The algorithm for sub-band DPD processing depends on this derivation for modeling PA output and spurious emissions. The processing for suppressing spurs is presented in the next section.

2.3 Sub-band DPD Processing

The decorrelation-based DPD training is generalized in this paragraph to easily explain the concept on a high level. Then, in subsequent paragraphs to this section, each part will be discussed in detail. Training begins by broadcasting through the power amplifier and receiving back the amplified signal. The spur of interest is then shifted in the frequency domain to be centered at baseband. We filter the signal to isolate the spur for training. A correlation is taken between the now isolated spur and the appropriate basis functions. An update to a DPD coefficient α is made to be the opposite of the magnitude and phase of the correlation. The α from this training is then convoluted with the basis function and added to the input. By doing this, we decorrelate the error signal from the basis function and minimize the spur.

With this sub-band DPD method, we hope to predistort by injecting a signal that will cancel the IMD signal seen in equation 2.3. This injection must be at the spur, so it will be frequency shifted from baseband to the proper location. For example,

the proposed injection signal for canceling the IM3 distortion seen in 2.9 would be such that the new composite baseband signal $\tilde{x}$ would be as follows in Equation 2.10.

$$\tilde{x}(n) = x(n) + \left[\sum_{\substack{p=3 \\ p \text{ odd}}}^{Q} \alpha_{3+,p,n} \star u_{3+,p}(n) \right] e^{j2\pi \frac{3f_{IF}}{f_s} n} \tag{2.10}$$

We must find α that decorrelates the observed spur or error signal, e, with the basis functions u. The value for α is calculated iteratively using a normalized least-mean square (NLMS) adaptive training algorithm. This is shown later in Equation 2.17. Before we present it, we must develop the notation.

Firstly, we construct a vector for the basis functions of a spur. If we consider up to a nonlinearity order of Q, we create a column-vector where each element is the nth sample for each odd, nonlinearity order p from 3 to Q. This is shown in Equation 2.12 for the IM3+ spur.

The basis functions are generated from the model. However, if each basis function is thought of as a vector consisting of all its samples, it is clear that each one has a projection on the other. They are not orthogonal and therefore to improve the stability of the convergence, the basis functions should be orthogonalized to each other.

Possible methods include QR decomposition. However, this requires that the entire basis function is known ahead of time. This is possible for the scenarios shown in WARPLab, but not for a real-time design. Instead, we propose a method that is more friendly for hardware. We will orthogonalize basis functions by subtracting the projection of higher order basis functions onto lower order basis functions. This is shown in Equation 2.11.

$$x_{IM3,5}(n) = x_{IM3,5}(n) - (x_{IM3,5}(n) \cdot x_{IM3,3})(x_{IM3,3}(n)) \tag{2.11}$$

This method reduces the orthogonalization process to be a scalar multiply and a element-wise subtraction. This method could trivially be pipelined in a hardware design without need for knowing the entire basis functions ahead of time. However, this assumes that the dot product of the two basis functions is known. It can be shown that this is deterministic based on the signal parameters. In a hardware implementation, this could be implemented by a look-up table.

Once the basis functions are orthogonalized, we build a similar vector to the previous one in Equation 2.12 where the orthogonalized basis functions are given as $s(n)$ with subscripts similar to earlier. This is presented in Equation 2.13.

To be able to correct for memory effects in the power amplifier, it is necessary to account for past values of the basis functions. To do this, we vertically append are previous vector with past values. This is given as Equation 2.14 where we consider memory effects for up to N values.

$$\mathbf{u}_{3+}(n) = [u_{3+,3}(n)\ u_{3+,5}(n)\ \ldots\ u_{3+,p}(n)\ \ldots\ u_{3+,Q}(n)]^T \qquad (2.12)$$

$$\mathbf{s}_{3+}(n) = [s_{3+,3}(n)\ s_{3+,5}(n)\ \ldots s_{3+,p}(n)\ \ldots\ s_{3+,Q}(n)]^T \qquad (2.13)$$

$$\bar{\mathbf{s}}_{3+}(n) = \left[\mathbf{s}_{3+}(n)^T\ \mathbf{s}_{3+}(n-1)^T\ \ldots\ \mathbf{s}_{3+}(n-N-1)^T\right]^T \qquad (2.14)$$

With these basis functions, we construct similar vectors for the DPD coefficients, α. Each orthogonalized basis function $s(n)$ will train a corresponding α that will construct its FIR filter taps for the predistortion. Each α will have N memory taps. Firstly, we construct the vector where each element corresponds to a different nonlinearity order up to order Q for delay tap l as in Equation 2.15. Secondly, we vertically concatenate the vector with similar vectors to account for all N delay taps

as in Equation 2.16.

$$\boldsymbol{\alpha}_{3+,l} = [\alpha_{3+,3,l}(n) \; \alpha_{3+,5,l}(n) \; \dots \alpha_{3+,p,l}(n) \; \dots \; \alpha_{3+,Q,l}(n)]^T \tag{2.15}$$

$$\overline{\boldsymbol{\alpha}}_{3+} = \left[\boldsymbol{\alpha}_{3+,0}(n)^T \; \boldsymbol{\alpha}_{3+,1}(n)^T \; \dots \; \boldsymbol{\alpha}_{3+,N-1}(n)^T\right]^T \tag{2.16}$$

With this notation, we preset the learning algorithm in Equation 2.17. In this equation, μ is a LMS gain parameter, and C is a constant to avoid errors due to small values of $\mathbf{s}(n)$. The equation is mostly the complex multiplication of the basis functions and the conjugate of the error signal observed by the receiver, $e(n)$. This gives a correlation between the basis functions and the error. By subtracting this from the previous value for $\boldsymbol{\alpha}(n)$, we move the coefficients in the opposite direction of the correlation. This method decorrelates the basis functions and the error signal which results in reducing the magnitude of the spur.

$$\overline{\boldsymbol{\alpha}}(n+1) = \overline{\boldsymbol{\alpha}}(n) - \mu \frac{\overline{\mathbf{s}}_{3+}(n)e^*_{3+}(n)}{\|\overline{\mathbf{s}}_{3+}(n)\|^2 + C} \tag{2.17}$$

Our composite baseband input signal can now be represented by Equation 2.18 where we have the input signal without DPD added to our predistortion injection signal at the frequency of the spur. The injection signal can be calculated by Equation 2.19.

$$\tilde{x}(n) = x(n) + \tilde{x}_{3+}(n)e^{2\pi j \frac{3f_{IF}}{f_S}n} \tag{2.18}$$

$$\tilde{x}_{3+}(n) = \overline{\boldsymbol{\alpha}}(n)^T \overline{\mathbf{s}}_{3+}(n) \tag{2.19}$$

To obtain the error signal $e(n)$, we must observe the actual content of the spur. We use a feedback training filter to isolate the contents of the error signal for the NLMS algorithm from the rest of the output. The power amplifier signal is shifted

in the frequency domain so that the center of the spur is at 0 Hz in baseband. Then, a least-squares FIR filter is used. This type of filter is preferred for a hardware implementation over a Parks-McClellan filter or others in that the real and imaginary components of complex data can be filtered separately and have the correct result as if the complex data itself was filtered. Moreover, a least-squares filter minimizes the $L2$ norm which by Parseval's theorem minimizes the energy of the signal. This is presented in Equation 2.20 for the IM3+ spur.

$$e_{3+}(n) = \text{LPF}\left(y(n)e^{-2\pi j\frac{3f_{IF}}{f_s}n}\right) \tag{2.20}$$

The methods in this section easily can be used for any spur by appropriately swapping out the basis functions and changing the frequency shifts.

2.3.1   Block-based Method

In [27], the third order version of this DPD algorithm was developed to train on a sample-by sample basis. However, this may not be practical in a real-time system. In a real system, when an update is made to $\overline{\alpha}$, it will be used to compute the injection signal. The injection signal will be applied to the input signal. Then it is written to a digital to analog buffer. From here, the sample will be converted to analog, sent to the upconverter, amplified by the PA, received and attenuated, downconverted, then sent to a analog-to-digital converter where it will then be sent to a buffer. Once the sample is read from the buffer, there is some latency for the calculations associated with Equation 2.17. It is clear that this entire path from injection to correlation will take many samples. It is essential to account for this loop delay in any control system. If loop delay is not accounted for, then updates made to α will not effect $e(n)$ until later. This can cause overshoot which may lead to instability. To correct for this, we introduce a block-based method originally presented in [34].

Blocks of length $L+P$ are broadcast into the power amplifier. The first L samples in what we call the "Learning Block" are used for training the next update to the DPD coefficient, α. We then apply the update the α being used in the predistortion. The update to α propagates thought the system, so we wait for P samples corresponding to our "Padding Block." For stability, it is necessary to have that $P > d$ where d is the loop delay in a system. We illustrate this is Figure 2.3.
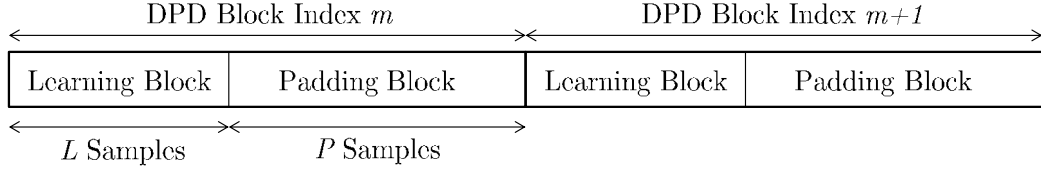

Figure 2.3: Illustration of block-based DPD concept

We generalize the previous equations to fit this structure. For Equation 2.14. we add L columns to correspond to the L samples in the learning block in a block with index m. This is shown in Equations 2.21. For α, we simply restructure it to be a function of the block index, m, instead of each sample. This is shown in 2.22. We similarly must make a vector corresponding to the error signal over the L samples in the learning block. This is shown in Equation 2.23.

$$\mathbf{S}_{3+}(m) = [\bar{\mathbf{s}}_{3+}(n_m) \; \bar{\mathbf{s}}_{3+}(n_m + 1) \; \dots \; \bar{\mathbf{s}}_{3+}(n + M)] \tag{2.21}$$

$$\overline{\boldsymbol{\alpha}}_{3+}(m) = \left[\boldsymbol{\alpha}_{3+,0}(m)^T \; \boldsymbol{\alpha}_{3+,1}(m)^T \; \dots \; \boldsymbol{\alpha}_{3+,N-1}(m)^T\right]^T \tag{2.22}$$

$$\mathbf{e}_{3+}(m) = [e_{3+}(n_m) \; e_{3+}(n_m + 1) \; \dots \; e_{3+}(n_m + L)]^T \tag{2.23}$$

With this, the learning is updated to be Equation 2.24.

$$\overline{\boldsymbol{\alpha}}(m + 1) = \overline{\boldsymbol{\alpha}}(m) - \mu \frac{\mathbf{S}_{3+}(m)\mathbf{e}_{3+}^*(n)}{\|\mathbf{S}_{3+}(n)\|^2 + C} \tag{2.24}$$

WARPLAB

A large component of the work done in this thesis uses WARPLab. WARPLab is an extension to MATLAB that allows for for rapid physical layer (PHY) prototyping on a software-defined-radio (SDR) board. This is a great method for doing initial testing before designing a dedicated FPGA circuit. Therefore, the various experiments done in this section are done with two intentions. Firstly, we explore various parameters in the algorithm and how they affect performance. Secondly, we perform experiments directly designed to help make the best design choices for the FPGA implementation development in Chapter 4.

3.1 Development Overview

We developed a WARPLab version of the algorithm originally presented in [38] and extended on in [34]. The most early work that was originally done used WARPLab version 7.4. However, everything has been upgraded to be completely compliant and compatible with WARPLab version 7.7 which is the latest version at the time of writing this thesis. All results shown in this thesis use this version.

The experimental set up and architecture is as shown in Figure 3.1. There is a

WARPv3 board connected to a PC running MATLAB via an Ethernet cable. The "RF A" port is connected to the "RF B" port via a 50 ohm coaxial cable with a 40 dB attenuator in-line.
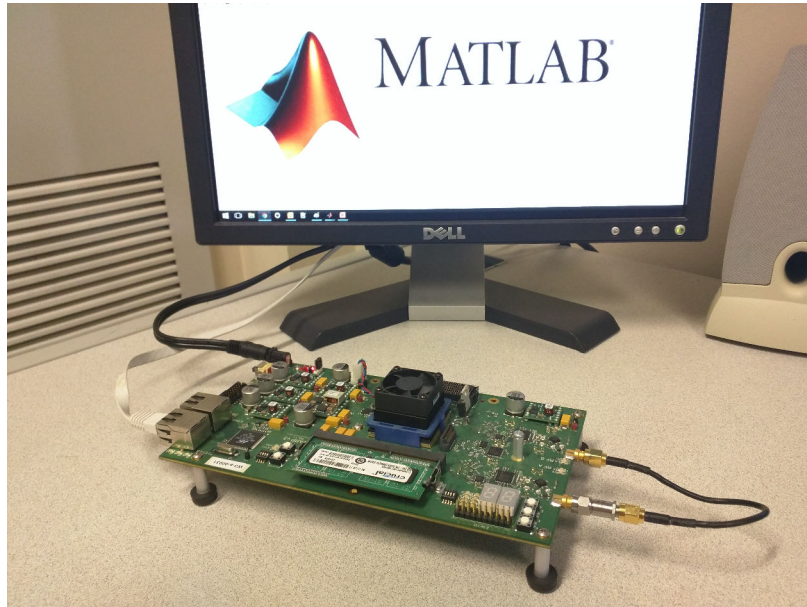

Figure 3.1: WARPLab Experimental Setup.

When performing spectrum analyzer experiments, previously trained coefficients are stored and used. The "RF A" port is connected directly to the spectrum analyzer. This set up is shown later in Figure 3.7.

3.1.1 Issues

When using a software-defined-radio (SDR) platform, it becomes apparent that there are many differences when using real hardware as opposed to doing simulations. The first issue that had to be overcome was time synchronization. By time synchronization, we mean coordinating a received sample on the WARP board to a transmitted sample. The delay seen from the start of a transmission to receiving the same information back is due to the analog components in the signals path. After a sample is

sent from the transmit buffer, it must go through the D/A, baseband processing, up-conversion, amplification on the transmit side. It then must go through attenuation, downconversion, baseband processing, and the A/D on the receiver side before the sample can be added to the receive buffer.

To properly account for this, a preamble is sent for a preliminary transmission when the board starts. This preamble is a standard STS and LTS preamble and is provided in the WARP OFDM example code. It uses an autocorrelation to find the start of a packet. With the WARP platform, the delay seen between transmitting and receiving is often about 43 samples. This value found by the autocorrelation at the beginning of an experiment is then used for the entire experiment.

By throwing out the initial samples for each broadcast based off the LTS, we choose the best sample to coordinate our inputs and output. However, this is not a perfect time synchronization. It is important to note that the analog components are not clocked and therefore there is no way to guarantee that data transmitted will be sampled by the A/D at exactly the proper time to perfectly coordinate with the transmitted data. It is very likely that there will be a subsample delay present [39]. For our purposes, this is typically not an issue and is not corrected. However, it is worth noting that this will manifest as a linear phase shift depending on the frequency.

The second major issue is phase. Once we know which received sample corresponds with which transmitted sample, it is quickly obvious that there is phase difference between the samples. Although the phase-locked-loops (PLLs) between the transmitter and receivers keep the phase noise between the two low, there is still a constant phase shift. It is necessary to correct this. We use a standard method to do so. The FFT of the input and output is taken and the output vector is divided by the input vector to return the average phase.

There is also an issue with a DC offset when transmitting. This is particularly noticeable when sending non-contiguous signals as the carrier leakage may intermodulate with the other component carriers to create additional spurs. To correct this, it was necessary to find an appropriate DC offset to apply for every transmission for each board. This was done simply by brute force.

3.2 Characterization of the WARP PA

In Figure 3.2, we plot output magnitude versus input magnitude for a LTE uplink signal with two 1.4 MHz carriers spaced 6.67 MHz apart. A total of 50k points are shown in this plot. The magnitudes are unitless quantities here. The input was scaled to be so that the inputs are always in the interval [-1 1] to accommodate the 12.11 fixed point precision expected for the DAC.

On this same plot, we include a nonlinear least-squares fit to this data. To create this model of the WARP PA, we use the statistical software R [40]. This model is based on equation 2.3 and includes up to ninth-order nonlinearities without memory. The resulting coefficients are in equations 3.1 - 3.5. The plot is generated by sweeping the real part of x from 0 to 0.6.

$$f_{1,1} = 3.8346 - 0.2541i \tag{3.1}$$

$$f_{3,1} = -19.5753 + 7.3116i \tag{3.2}$$

$$f_{5,1} = 43.6597 - 66.4488i \tag{3.3}$$

$$f_{7,1} = 11.9489 - 202.7031i \tag{3.4}$$
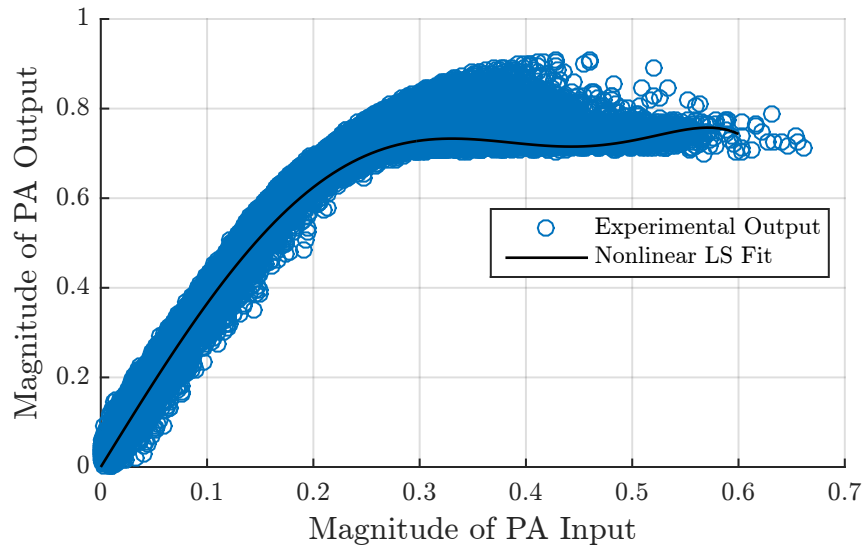
$$f_{9,1} = -106.0553 - 204.1277i \tag{3.5}$$

Figure 3.2: PA Output vs. PA Input for a LTE uplink signal with two 1.4 MHz carriers spaced 6.67 MHz apart with the WARP board broadcasting at a high gain and a nonlinear least-squares fit to the data.

For magnitudes less than 0.3, we see a mostly linear behaviour. However, beyond that point, the PA appears to be in saturation. It is not able to provide more power for the larger magnitudes. For this test, we also verified that the maximum values for the real and imaginary parts were less than 1 to be sure that what we see is PA saturation and not ADC saturation.

3.3 3rd order IM3 DPD

The most early work performed in WARPLab was to simply suppress the third order nonlinearity in the IM3+ spur without accounting for memory effects. We present that work in this section.

In Figure 3.3 we show a general block diagram for this and subsequent experiments to illustrate where each part of the algorithm is done. We show a memoryless DPD

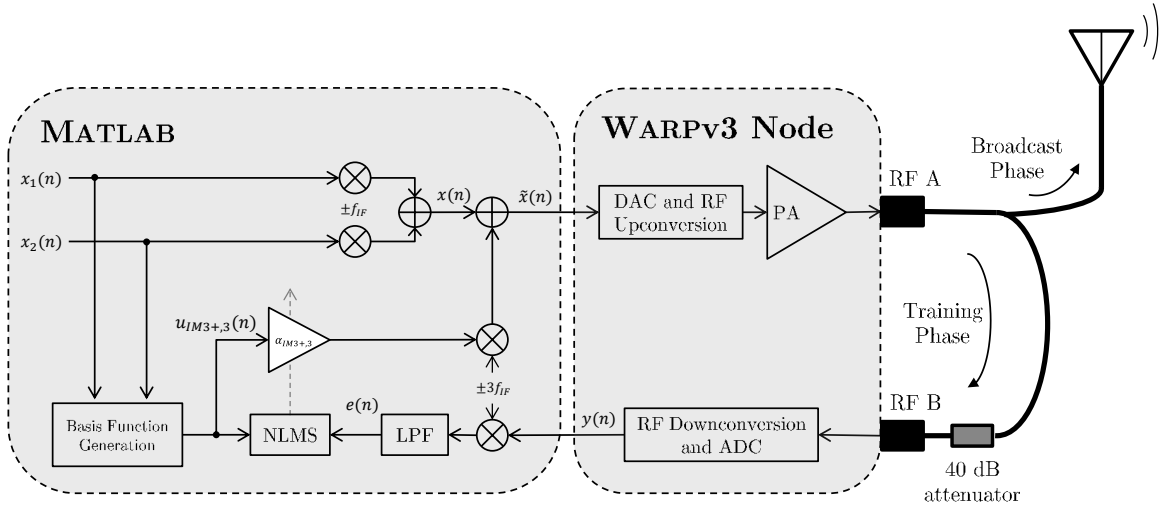algorithm with nonlinearity order Q.

Figure 3.3: WARPLab DPD architecture for third-order, memoryless implementation.

In Figure 3.4 we show a standard result for the WARPLab, 3rd order, IM3 DPD. The power spectral density is calculated relative to the strength of the main carriers in dB. This result shows approximately 15 dB of suppression. In Figure 3.5, we see a smooth convergence of the DPD coefficient α. For this example, the LMS gain, $\mu = 0.3$, the block length is 1024, and the learning block length is 528. There are two 1.4 MHz LTE uplink SC-FDMA carriers. The spacing between the carriers is set to 6.7 MHz.
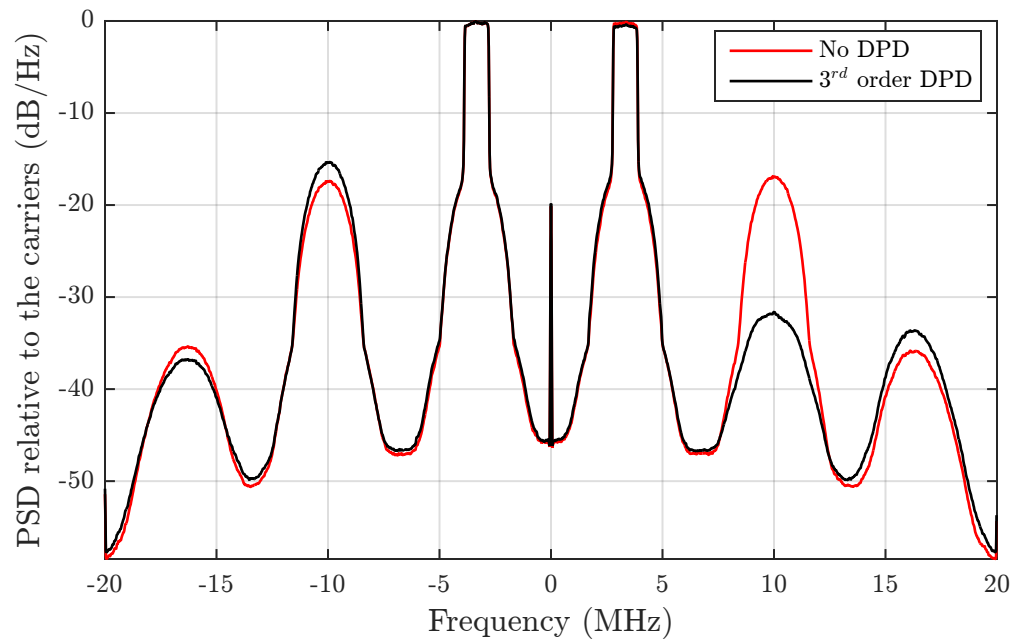
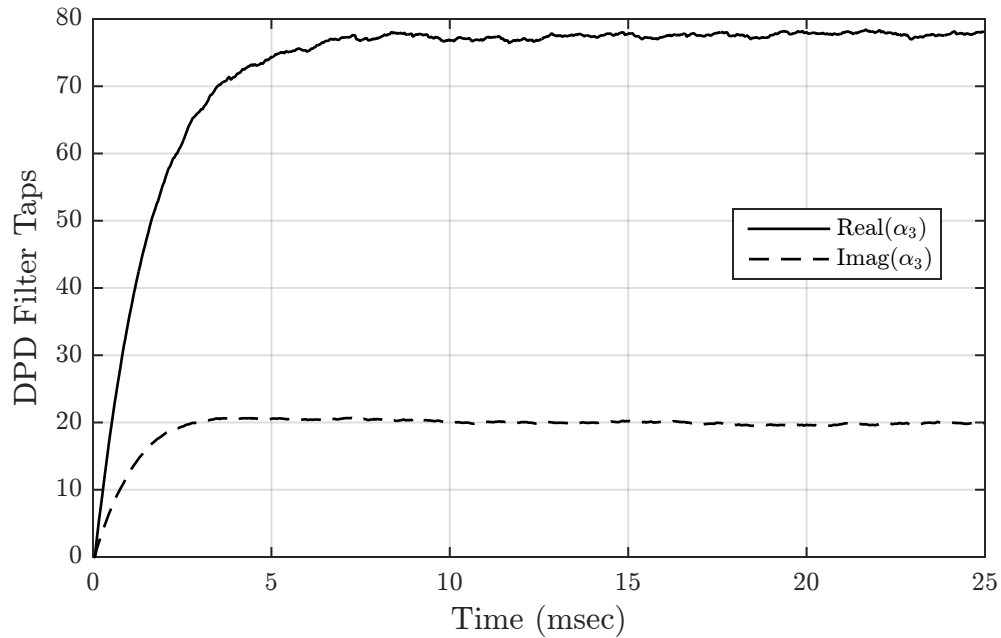Figure 3.4: Spectrum before and after 3rd order IM3 DPD suppression

Figure 3.5: Convergence of 3rd order IM3 DPD coefficient α

For Figure 3.6, the LTE signal with and without DPD using the final coefficients from figure 3.5 were broadcast statically using the continuous TX feature of WARPLab. The spectrum analyzer was set with a span of 40 MHz. The resolution bandwidth was 1 kHz. The video bandwidth was 300 Hz. The scale is so that there are 6 dB of suppression, so we can very clearly see approximately the same 15 dB reduction in IM3 power that is visible in Figure 3.4. This validates the results seen in MATLAB, so for most experiments, we will rely on the results from taking a spectrum in MATLAB. The experimental setup for this test is shown in Figure 3.7.
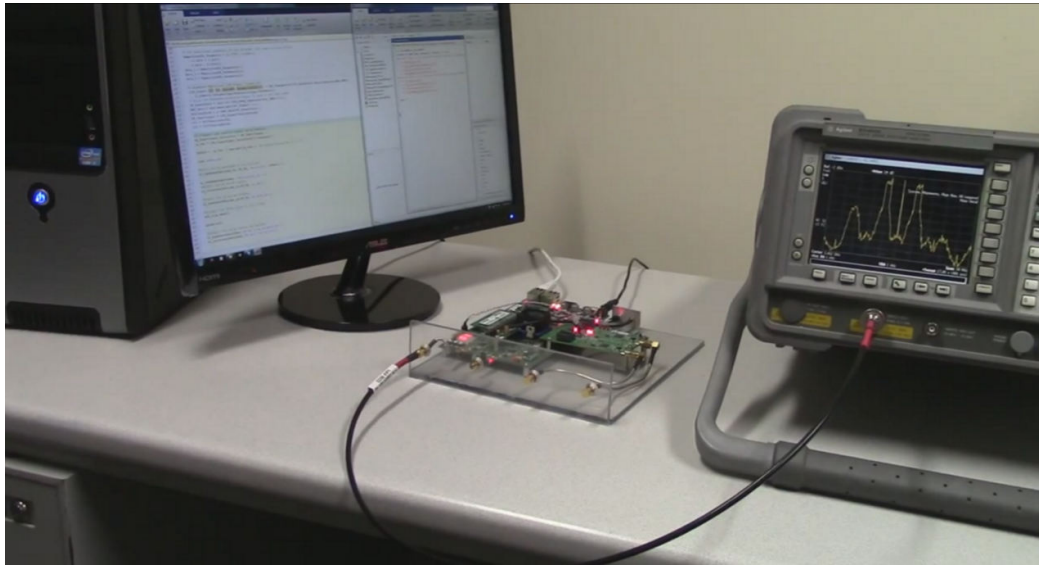
Figure 3.7: Experimental setup when testing with the spectrum analyzer.
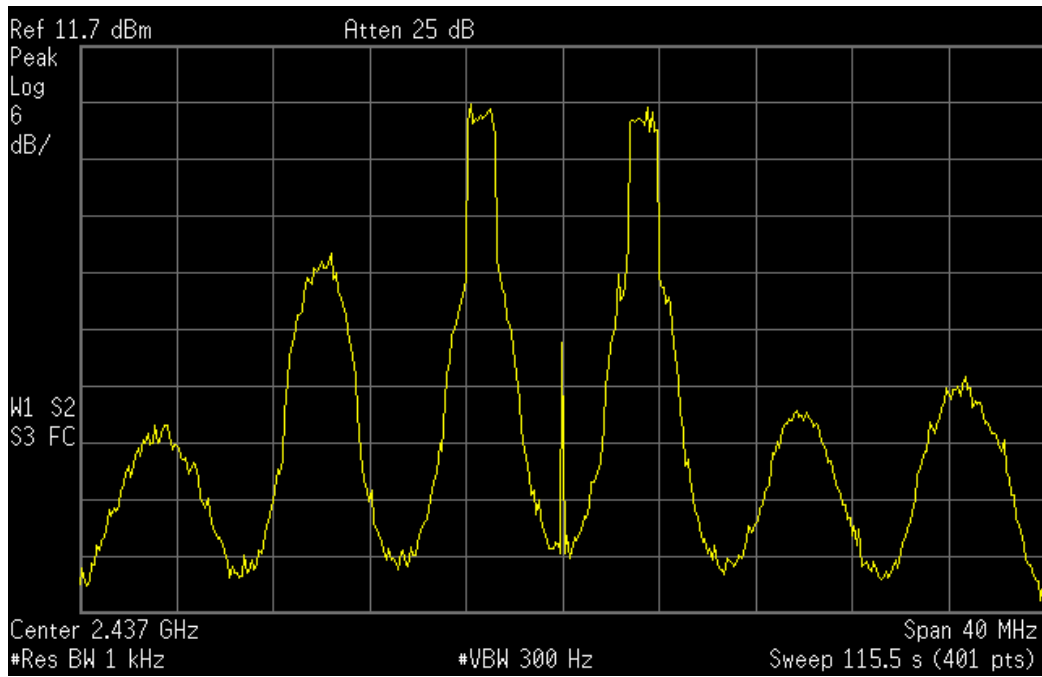

Figure 3.6: DPD result plotted using spectrum analyzer data

3.3.1 Lefthand IM3 Spur

The low-complexity algorithm presented in this paper is low-complexity in that we only target the most troublesome spurs instead of linearizing the entire signal. It is trivial to target the left-hand IM3- spur instead of the right-hand side as we have so far shown. To do this, we simply need to swap the component carriers in Equation 2.5. This result with and without DPD for the power-spectral density is shown in Figure 3.8 and its corresponding plot for the convergence of the DPD coefficient α is in Figure 3.9. When comparing this result to the IM3+ result presented previously in Figure 3.4 and 3.5. The IM3 suppression is virtually equivalent. The convergence for the DPD coefficient α is similar in that the convergence is smooth and is converging to similar numbers. For simplicity, most of the results beyond this will only show DPD for the positive baseband frequencies.
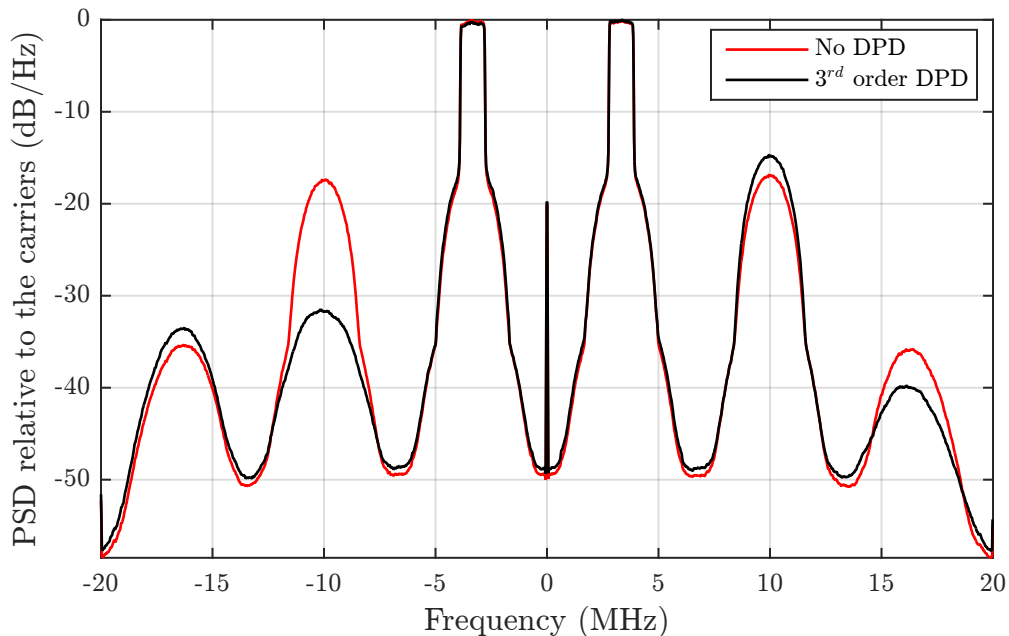

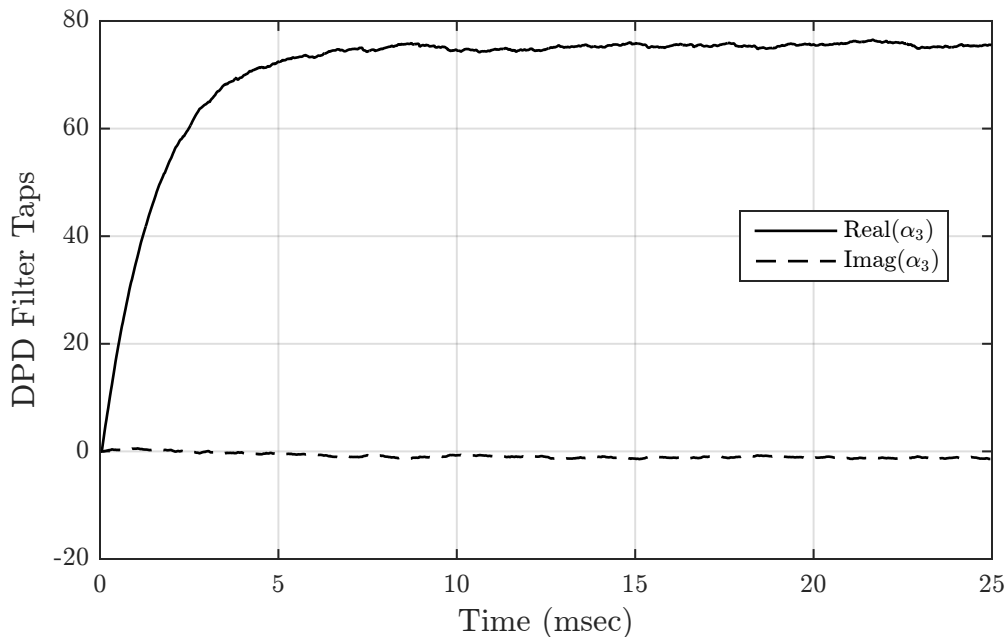Figure 3.8: Spectrum before and after 3rd order IM3- DPD suppression

Figure 3.9: Convergence of 3rd order IM3 DPD coefficient α

3.4 Higher Order IM3 DPD

From Equation 2.17 we develop the algorithm for suppressing higher-order nonlinearities. We show the spectral result in Figure 3.10 and the convergence of α in Figure 3.11. In the PSD, we show the reslut as we add on more nonlinearity terms. With each additional term, we see additional suppression. However, there are diminishing returns. The fifth order suppresses approximately an extra 5 dB while each additional order beyond that suppresses approximately an additional dB.

In the convergence plot, we see smooth convergence for all terms. The α_3 coefficient converges to a nearly identical value to what it does in the previous IM3 third order convergence plot from Figure 3.5. This is because of our technique of orthogonalizing higher order basis functions to lower order basis functions.
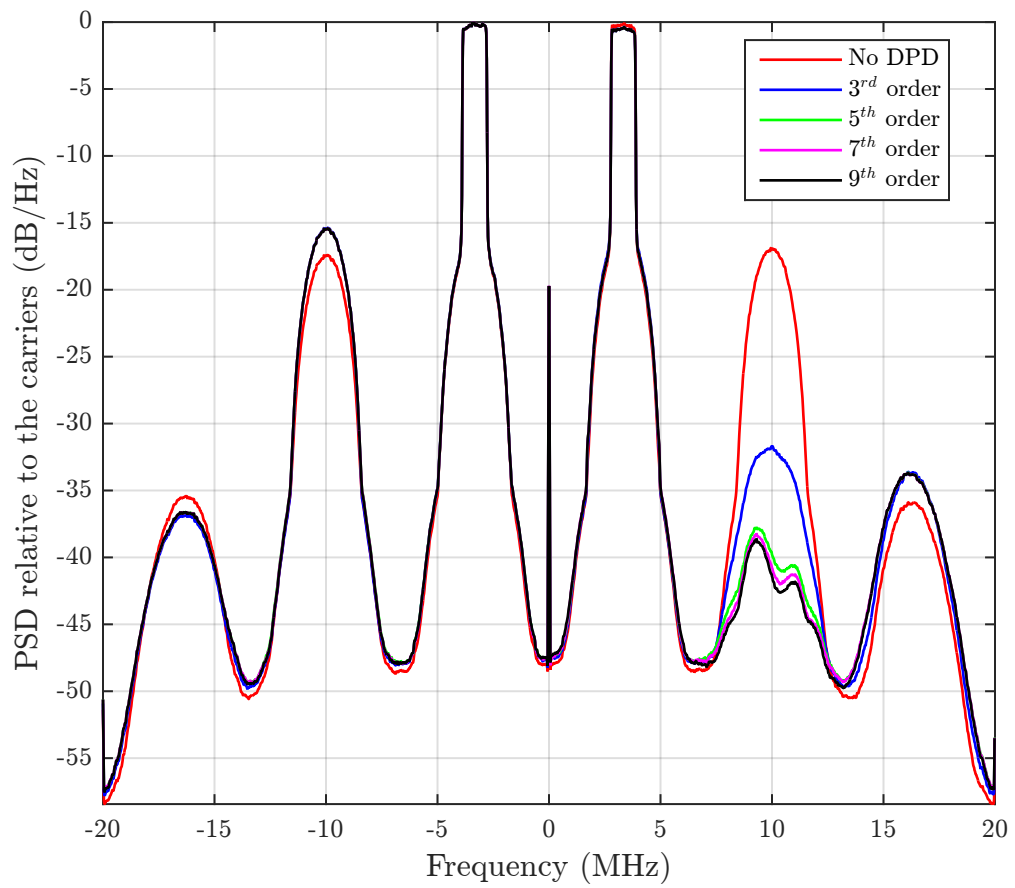
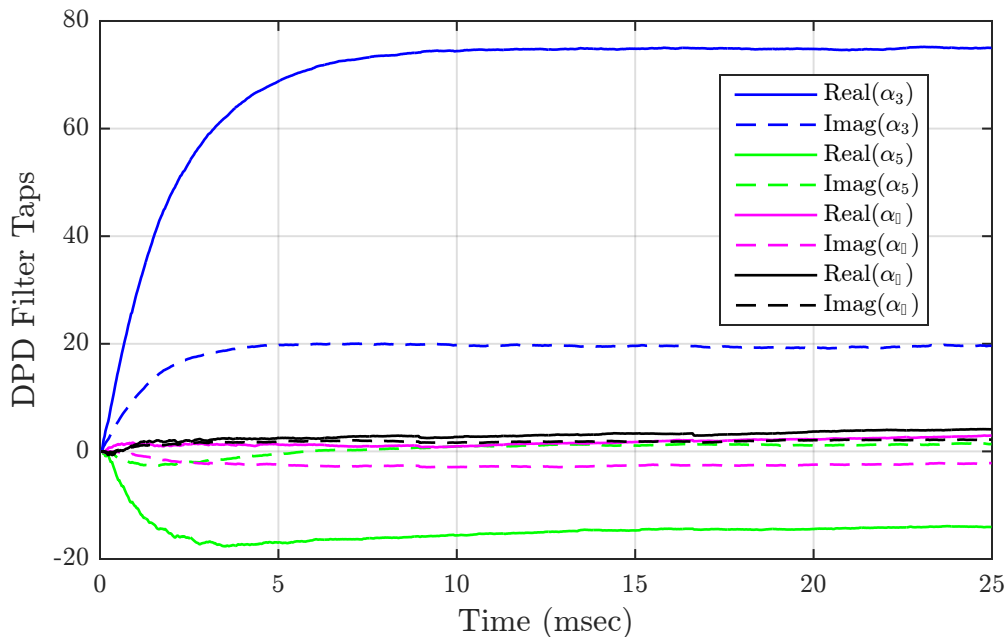Figure 3.10: Ninth Order IM3 Suppression

Figure 3.11: Ninth Order IM3 Convergence

3.5 Performance variations between WARP boards

For the purpose of consistency and control, we show all experiments with the same board (W3-a-00031). However, it is important to emphasize that our DPD methods are generalizable to different signal parameters and hardware. In this section, we show some of the robustness with respect to hardware by performing tests on two different WARP boards. For these tests, we keep all the signal parameters from the previous section constant. The only thing that changes with the board is the DC offset applied and the RX Gain settings if necessary to avoid saturating the ADC.

In Figure 3.12 we see the spectrum and the convergence for up to ninth order IM3 DPD on W3-a-00424. This board has extreme saturation effects as evident in the spectral plot. The relative height of each IM3 spur is -12 dB and only about 15 db of IM3 suppression is achieved. The coefficients converge smoothly and similarly to the other board. However it converges to a larger α. This is to be expected considering
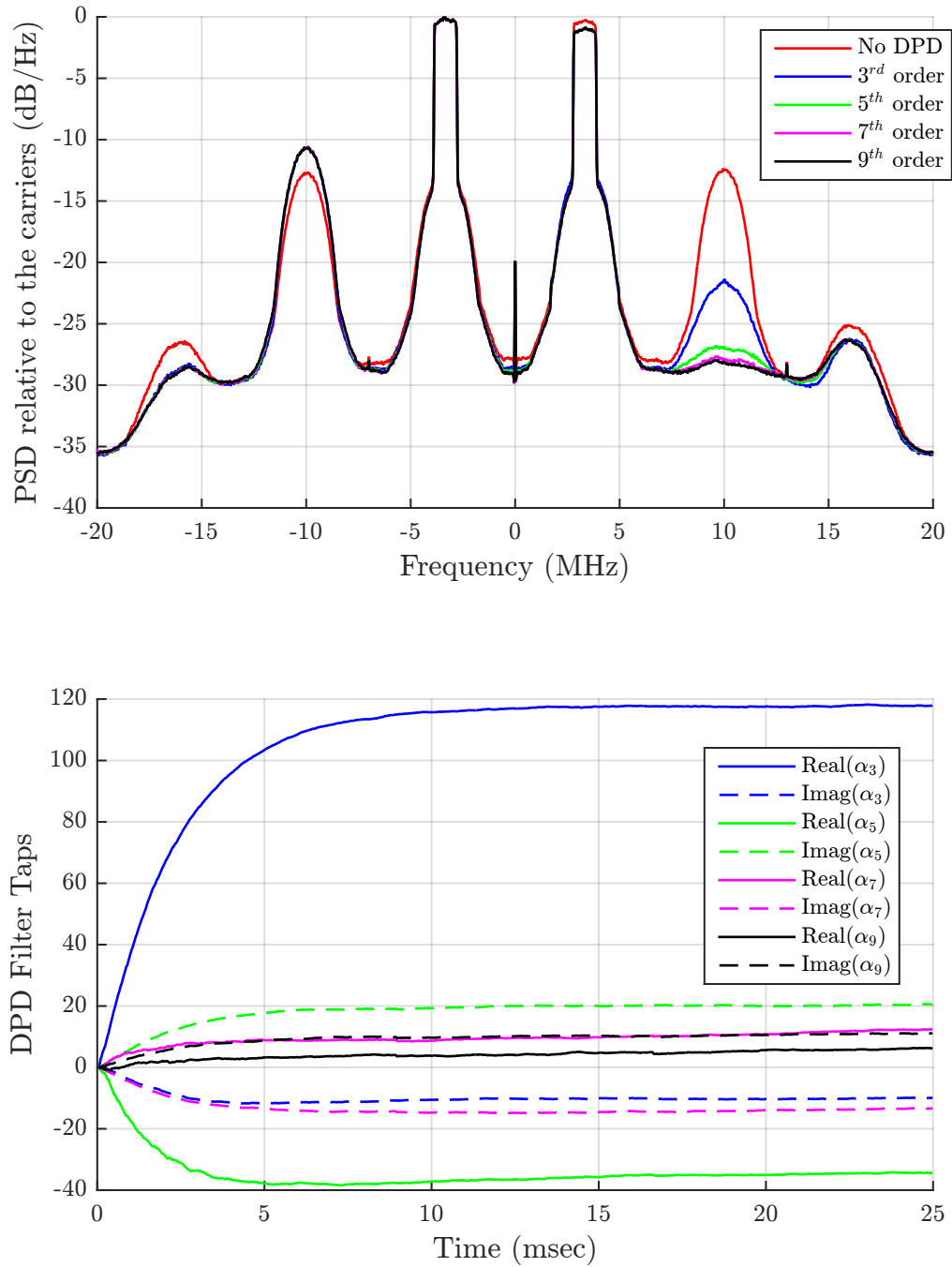
Figure 3.12: High Order Convergence for WARP Board 424

the magnitude of the spur.

In Figure 3.13 we see the spectrum and the convergence for up to ninth order IM3 DPD on W3-a-00595. This performance for this board is very much similar to the board that we use throughout the thesis for all the results. Coefficients again converge smoothly and to values similar to the other boards.

Although the three boards used have different characteristics, we see similar performance and ability for the algorithm. The coefficients all converge smoothly. We see that they converge to similar magnitudes with variations usually appearing in the imaginary part of the coefficients. All boards see at least 15 dB of suppression when using ninth-order DPD.

3.6   Memory based DPD

By adding additional "taps" to α for each nonlinearity order, it is possible to account for memory effects in the power amplifier by training α to have multiple memory taps. We do that in this experiment. For each order, the DPD coefficient is given a memory depth of two. In Figure 3.14, we see the spectrum after training with this memory-based DPD model. Here we see similar convergence to the earlier results with approximately 15 dB for third-order training and approximately 23 dB for higher-order training.
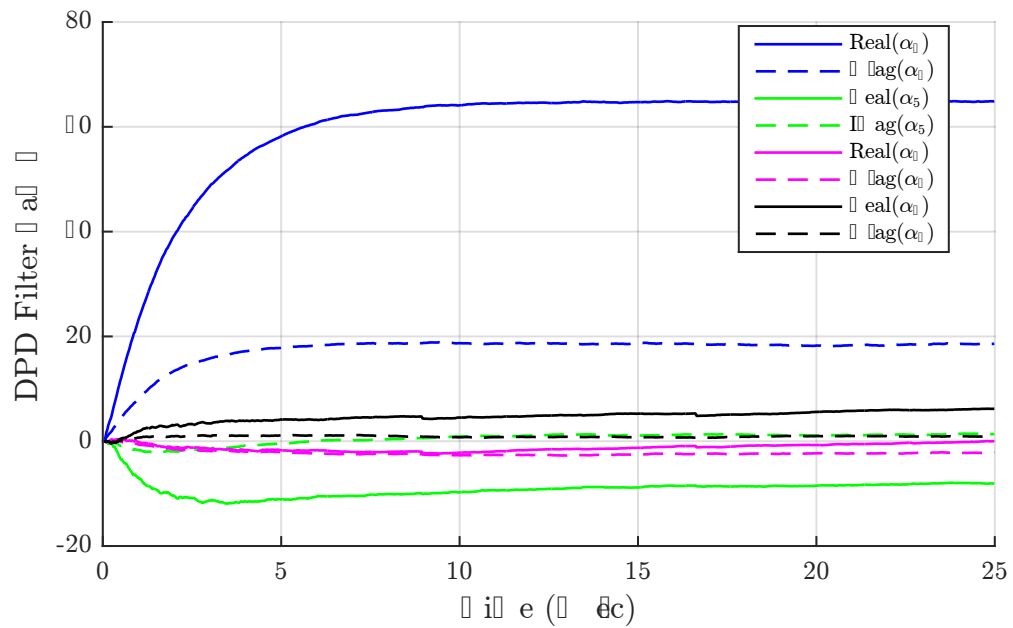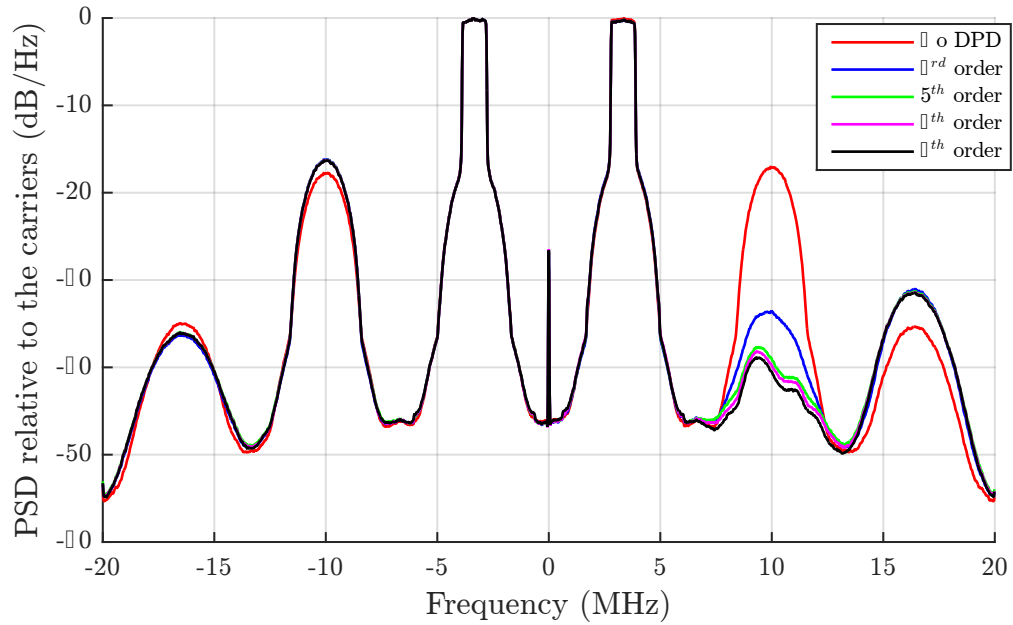
Figure 3.13: High Order Convergence for WARP Board 595
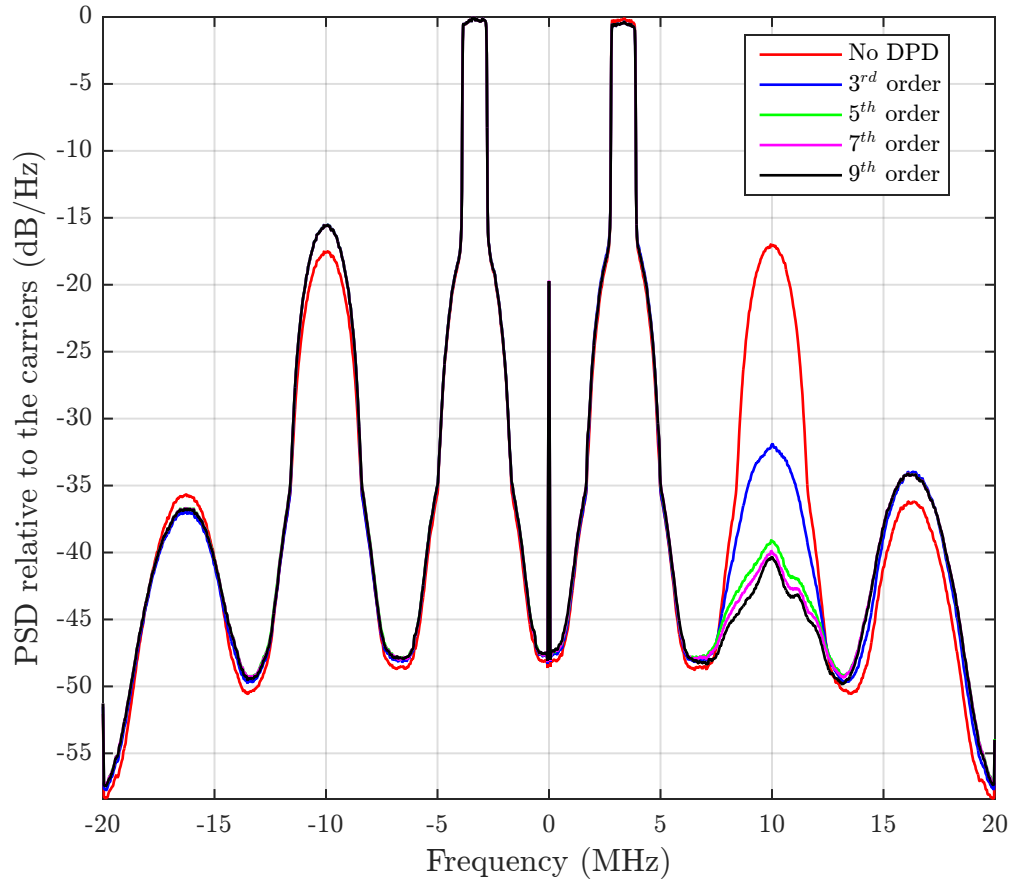
Figure 3.14: Memory based DPD Spectral Result

In Figure 3.15 we see the convergence for this type of DPD. For readability, the real and imaginary parts of each α where not included. Instead the magnitude is plotted for each tap of the predistorter. From the figure, we see smooth convergence of the coefficients. The dotted lines represent the second tap for each filter order.
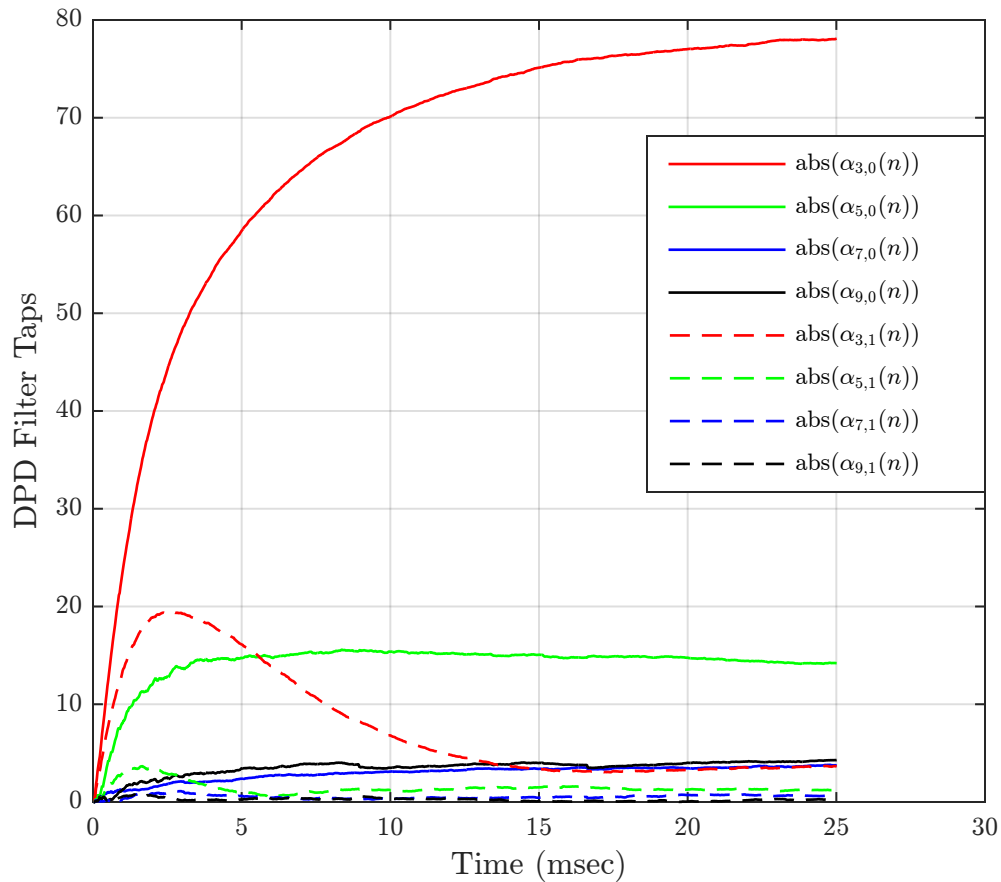
Figure 3.15: Memory based DPD Convergence Result

3.7 Larger Component Carriers

There is no scenario in LTE where there will be two 1.4 MHz carriers being aggregated on the same band [41]. All of the work presented here has been with 1.4 MHz carriers because it was more feasible for the limited bandwidth of the WARP platform and a reasonable initial test signal. To properly test these algorithms for LTE, a different platform would be ideal. However, additional testing was done on the WARP platform for 3 MHz and 5 MHz carriers. The next carrier size supported by LTE is

10 MHz. However, the sampling frequency of WARP is not high enough to support non-contiguous carrier aggregation.

3.7.1   Two 3 MHz Component Carriers

The 3 MHz is never used in the LTE specifications for non-contiguous carrier aggregation. However, it is possible to do in WARP, so testing was performed. We see that in Figure 3.16, performance is similar to the previous 1.4 MHz testing. There is approximately 15 dB of suppression for the third order DPD and approximately 20 dB for higher orders. In Figure 3.17, we see smooth convergence. The converged coefficient α is similar to the 1.4 MHz convergence shown for this board in Figure 3.11.

Figure 3.16: PSD plot when using larger carrier bandwidths of 3 MHz. Here, we see a similar 15 dB for the third order DPD and 20 dB for higher orders.

Figure 3.17: Plot of the convergence of all the DPD coefficients when using two 3 MHz carriers. Here we see that all the coefficients convergence smoothly and similarly to previous results.

3.7.2 Two 5 MHz Component Carriers

Using two 5 MHz component carriers is a more realistic scenario. In fact, this setup is compliant with many carrier aggregation scenarios including CA_2A-2A and CA_42A-42A [41]. The carrier spacing for the experiment was increased to 9 MHz. Without adjusting the carrier spacing to be larger as we have done, there would be overlap between the carrier regrowth, IM3, and IM5 spurs making convergence difficult.
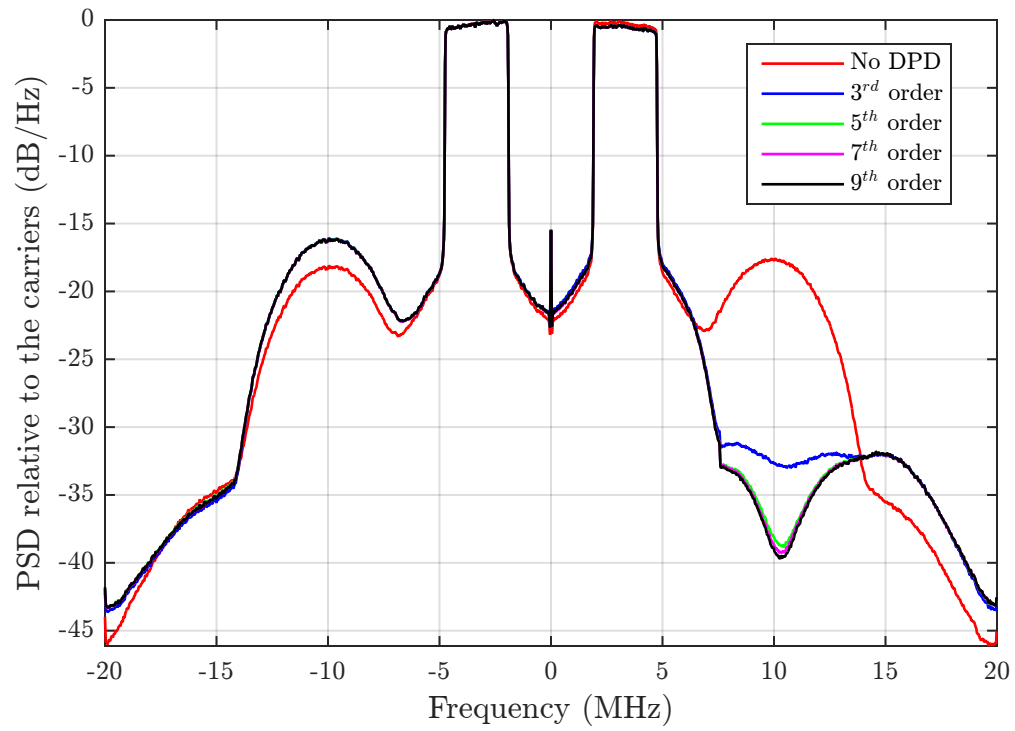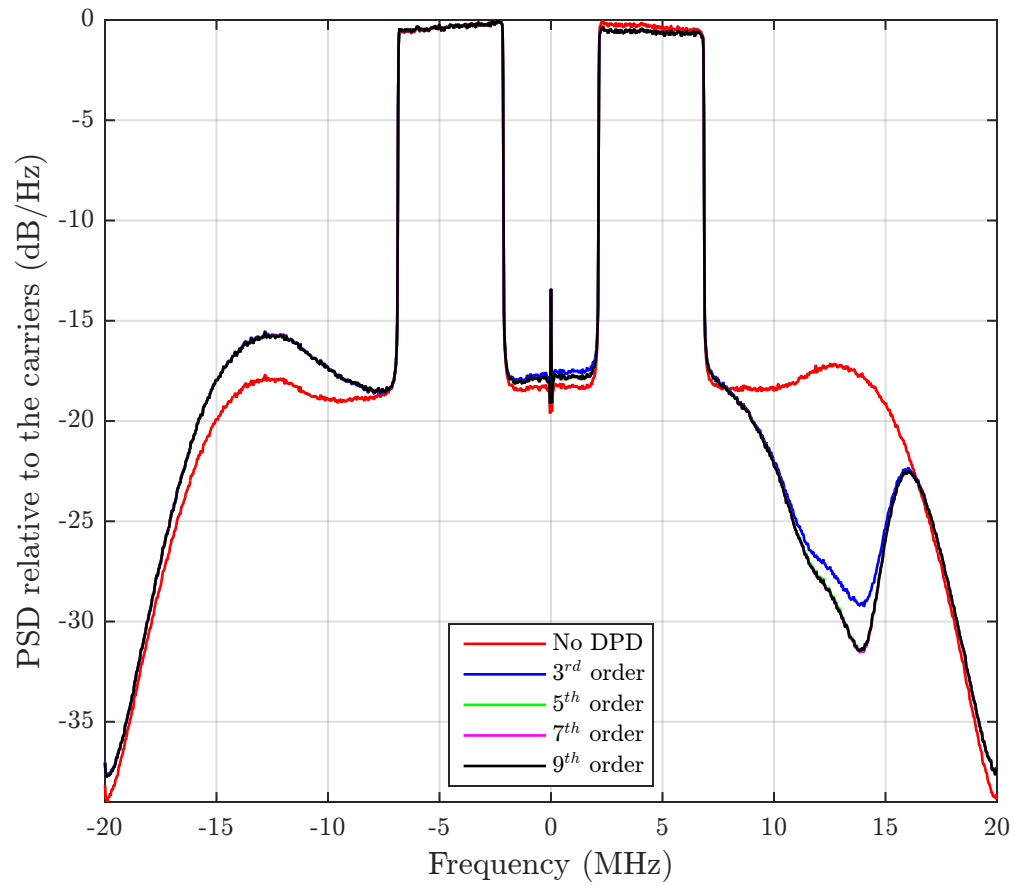
Figure 3.18: PSD plot when using larger carrier bandwidths of 5 MHz. Here, we see a similar ~15 dB for the third order DPD and ~20 dB for higher orders.
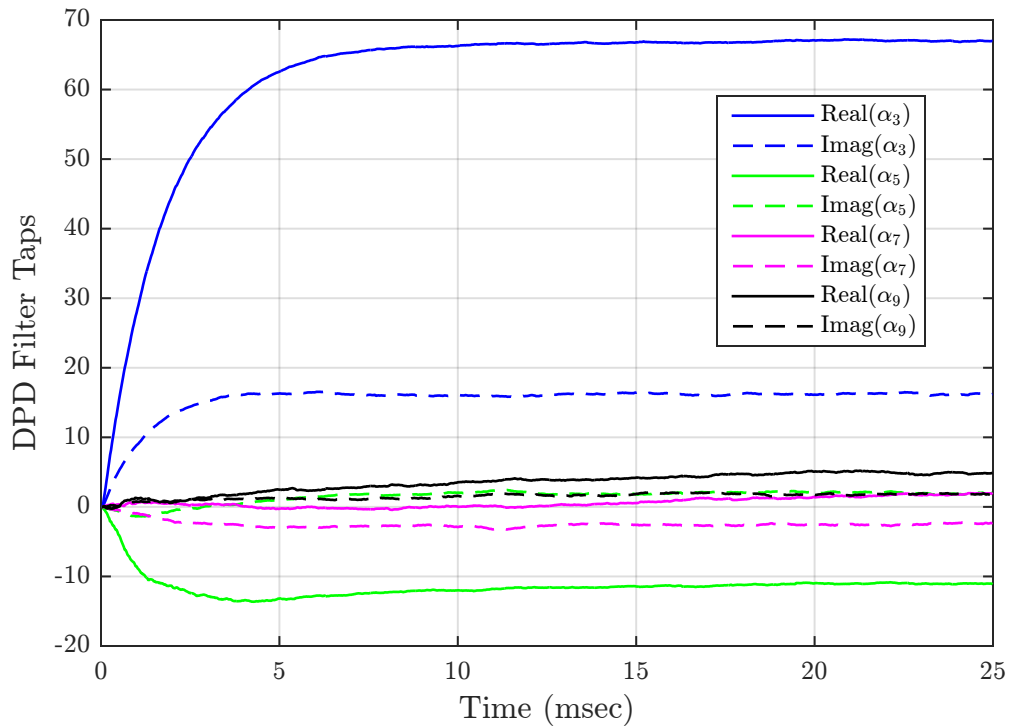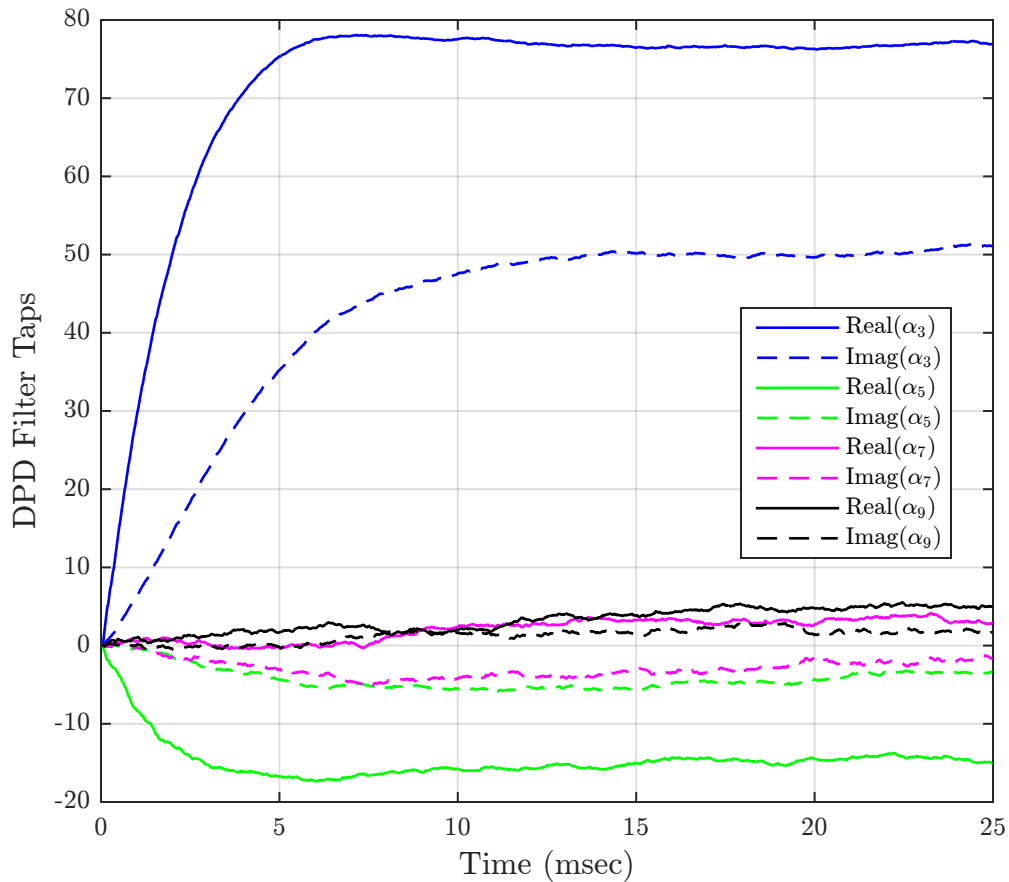
Figure 3.19: Plot of the convergence of all the DPD coefficients when using two 3 MHz carriers.

3.8 WURC-based UHF DPD

In this section, we examine the performance on a UHF system. This highlights the robustness in the algorithm and system by having it operate on an entirely different frequency band with entirely different hardware. This work is also interesting in that 700 MHz is used by multiple carriers for LTE in the United States and Sprint uses the nearby 850 MHz LTE band where carrier aggregation may be performed.

Experiments were conducted between 440 and 770 MHz. The WURC daughter card for WARP is used [42]. It uses a wideband Lime Microsystems transceiver [43]. In Figure 3.20 we show results for broadcasting at 550 MHz on this board while the gain is set to its maximum. DPD was only performed for third-order nonlinearities because the high noise floor for this board made attempting to compensate for higher orders futile. However, the coefficient converges smoothly and 10 dB of suppression is achieved.

The WURC daughter card for WARP has a WARPLab like infrastructure that is based on WARPLab 7.4. Being based on version 7.4, it does not utilize the DRAM of the board. Instead, samples are stored in BRAM. This significantly reduces the maximum transmission size. The PSD of Figure 3.20 was generated using the maximum transmission size of approximately 32k samples. Earlier PSDs were generated using much more samples. Hence, the PSD in 3.20 is less smooth than other plots.

3.9   Receiving on a Different Channel

The work thus far shows that the algorithm is capable of performing well on real hardware. However, there are many impracticalities with the system so far. Firstly, when using a non-contiguous carrier aggregation, it is probable that the carrier spacing will be larger than what has been used thus far. Smaller carrier spacings have been chosen to ensure that the IM3 spur fell within the TX/RX bandwidth.

To partially help to accommodate larger carrier spacings, the WARPLab implementation was modified so that the receiver would be tuned to a different frequency as the transmitter. This would allow for receiving directly on the spur of interest.

This method has many potential advantages beyond helping to accommodate larger carrier spacings. Firstly, by receiving directly on a spur, it is no longer necessary to shift the spur to baseband after receiving. By allowing the already existing
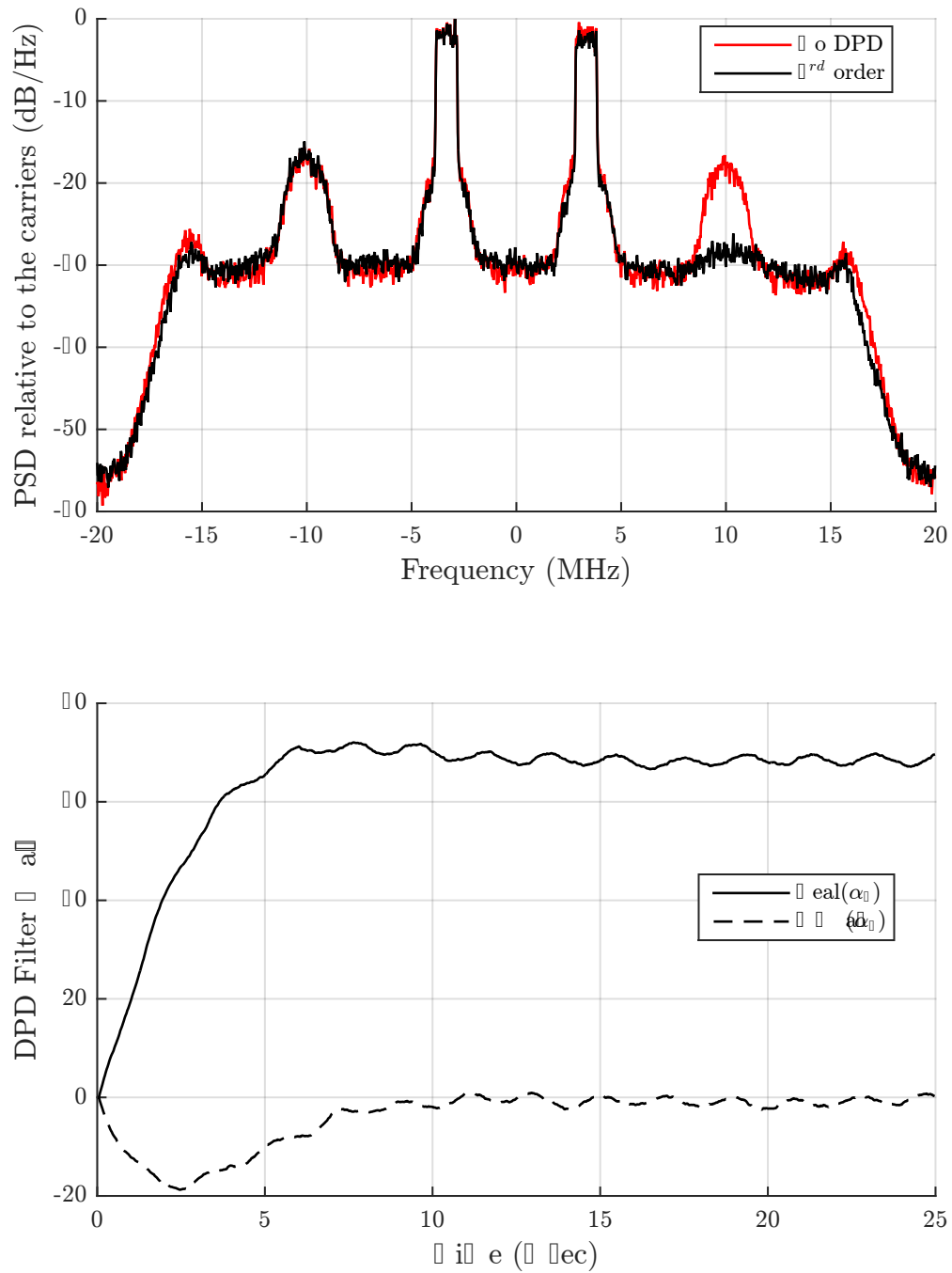
Figure 3.20: DPD on WURC UHF Board

hardware to do this work, the complexity is reduced by a complex multiply.

When receiving on the same channel as the transmitter, the receiver gain is limited by the main carriers as they will saturate the ADC before the IM3 spur as they are usually 15 dB stronger. By receiving on a different channel, the RX LPF filters can reduce the magnitude of the main carriers so that the ADC is not saturated and the gain can be increased. This can improve training especially for the higher order basis functions. The RX LPF can also be set more narrow than when transmitting and receiving on the same channel. By doing so, the order of the feedback FIR filter can be reduced. This again has the advantage of using the already present analog hardware to reduce the number of digital computations necessary.

For this experiment, we set the carrier spacing strategically. When the carrier spacing is set to 6.67 MHz, the IM3 spur is located at 10 MHz. This is convenient in that WARPLab allows the user to tune the transmitter and receiver to WiFi channels. Since Wifi channels are spaced every 5 MHz, we have placed the spur 2 channels over.

In Figure 3.21, we show the result of this technique. We see similar suppression of the IM3 spur compared to the earlier figure. In this figure, we also observe a new phenomenon. It appears that the primary component carriers are mirroring across the RX center frequency and appearing at lesser magnitudes on the IM5 and IM7 spurs. This is the result of IQ imbalance [44] and is not a problem for us.

In Figure 3.22, we see the convergence of the coefficients. The coefficients converge similarly to the previous figure as we would expect.
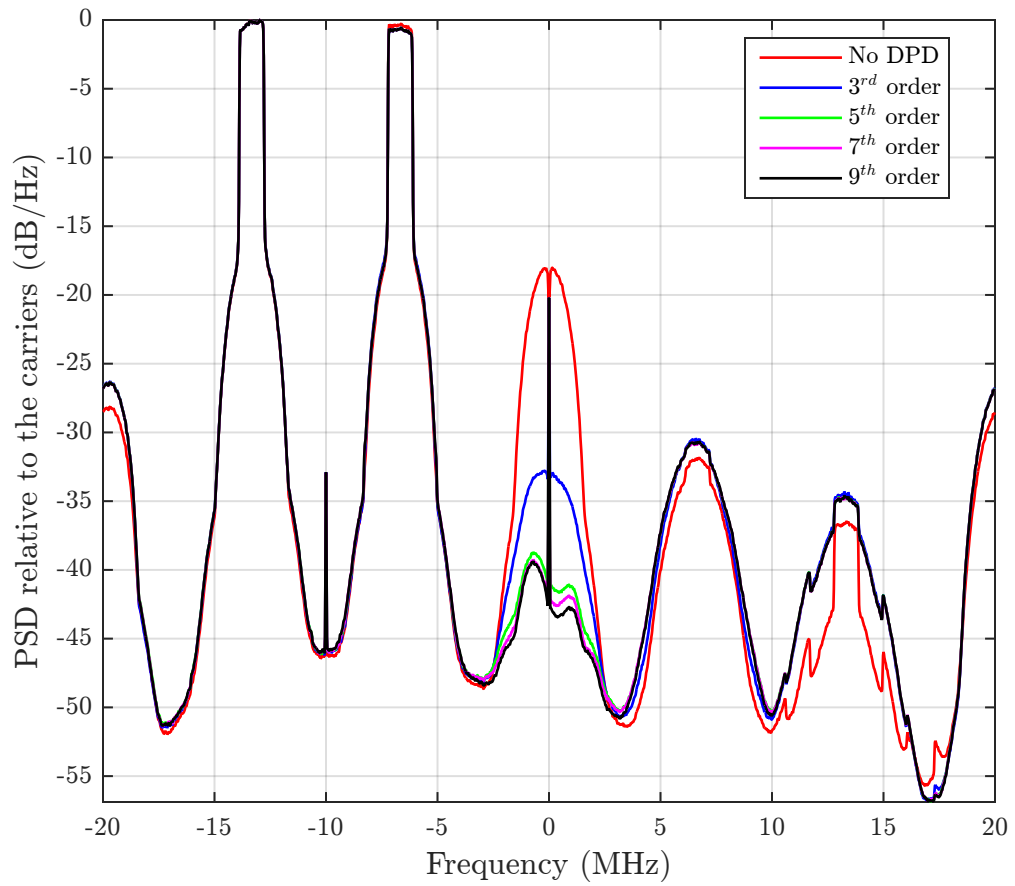
Figure 3.21: DPD PSD result for up to 9th order DPD when we TX and RX on different channels. Here, we can see similar results to shown earlier.
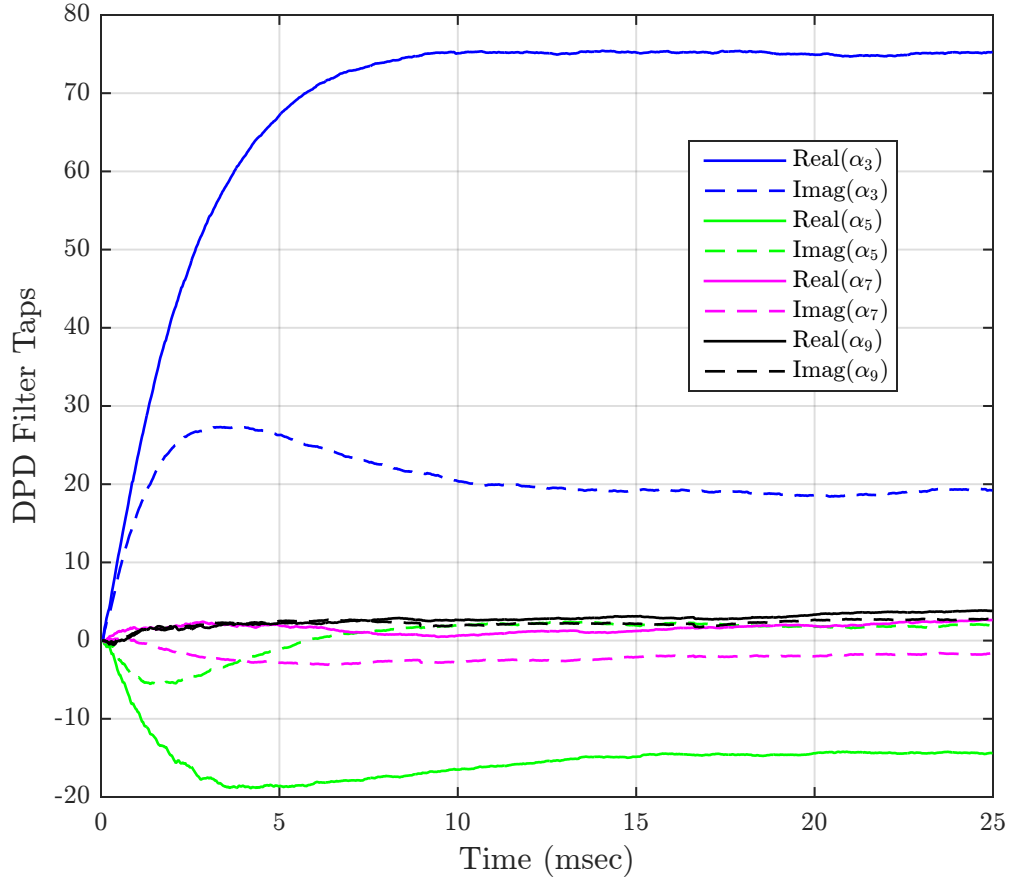
Figure 3.22: Plot of the convergence of all the DPD coefficients when TX and RX on different channels.

One difficulty is that even though there should be 5 MHz between channels, we find that there is some precision issues with the tuning. Using the CFR Fitz algorithm [45], we estimate there to be an additional 77 Hz that needs to be accounted for in the spacing estimate for the algorithm.

We also note that it is still necessary for predistortion that we are able to broadcast a predistortion spur at the targeted spur frequency. So through this technique, only the RX location constraint has been relaxed. Also, it is still necessary to phase

synchronize the transmitter and receiver. To do this currently, the receiver needs to be able to accurately observe the LTE component carriers. Hence, we are still constrained in the WARP system to smaller carrier spacings and bandwidths. This also makes it difficult to tighten the RX filters and increase the gain as we hypothesize could help. However, this is still an important step in the proper direction to a more flexible system.

3.10   Multiple Spurs

This work is targeted for scenarios where full-band DPD is excessive and there may only be one spur in violation. However, the techniques presented here can be applied to multiple spurs if necessary. For the experiment, we target the IM3+ and the IM3- spur.

As evident in all PSD figures presented so far, training one spur tends to have a negative effect on others. This is because our input signal is no longer simple x. It is now in essence a signal with 3 carriers. This extra carrier intermodulates with the others and contributes to other spurs. If one of these spurs goes above emissions standards, we can also train it.

We train the right side using up to ninth order basis functions. We then train the left side. When we do this, we see that it has a negative impact on our previous training. This is shown in Figure 3.23.
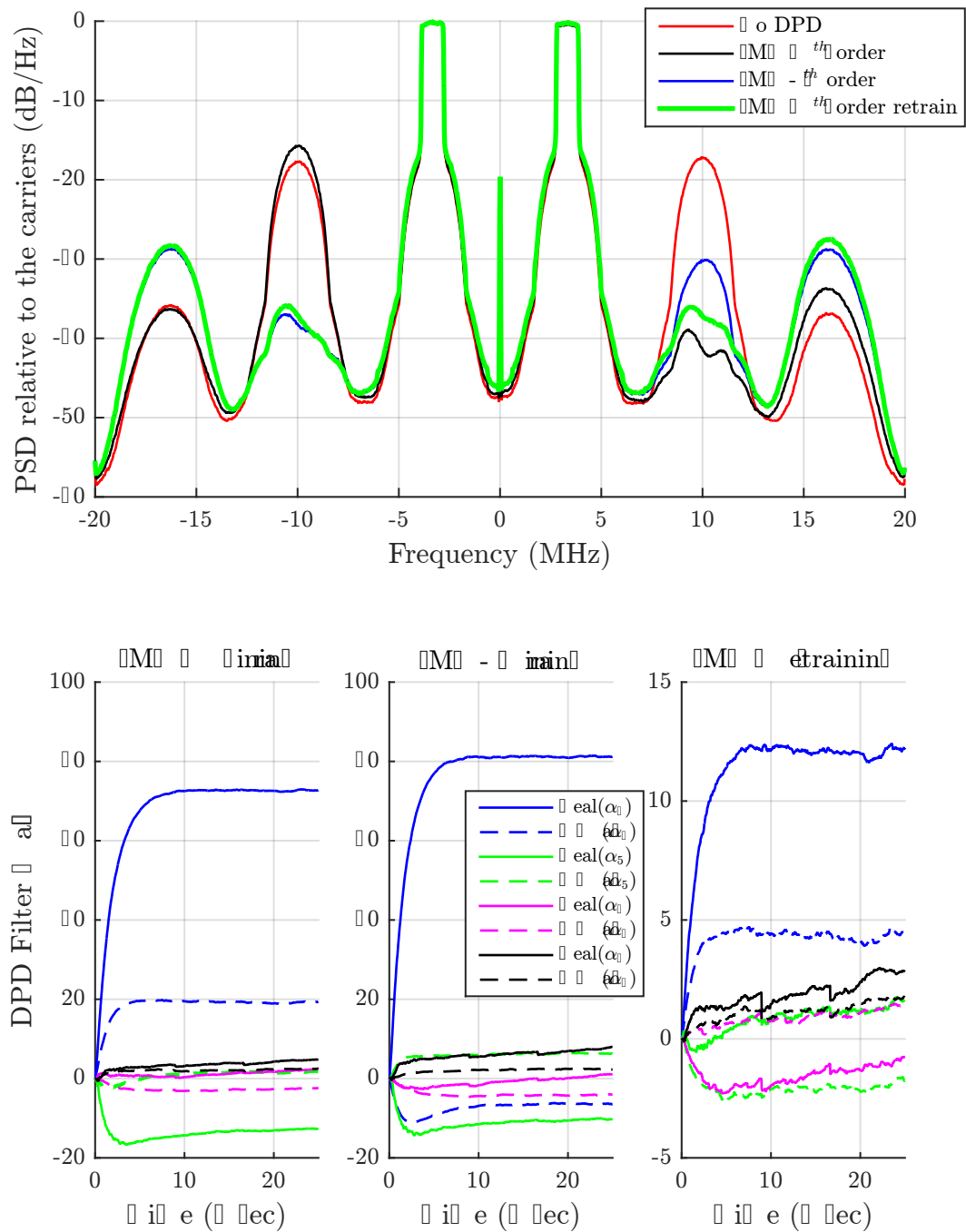
Figure 3.23: Here we train three times. For the first training period, we train for the IM3+ spur using ninth-order DPD shown in black on the PSD plot. Secondly, we train the IM3- spur again using ninth-order DPD. This is shown in blue on the PSD plot. This has a negative effect on the IM3+ spur so we retrain it. The final plot in green on the PSD shows after training a total of three times.

FPGA Design

The WARPLab prototyping provided valuable insight into the behaviour of a real power amplifier. However, WARPlab does not perform real-time testing. The end-goal of an algorithm such as the one tested in this thesis is implementation in a real system. We take the algorithm an additional step beyond a WARPLab prototype in this chapter and develop a field-programmable gate array (FPGA) based prototype. The FPGA design operates in real-time to predistort non-contiguous LTE transmissions and suppress the right-hand IM3 spur.

4.1 Development Overview

The FPGA design was created in Xilinx System Generator for DSP version 14.4 [46]. The ISE design suite edition version 14.4 was used [47]. MATLAB version 2015a was used to create LTE data, and the Simulink software hosted the System Generator tools. A Chipscope core was used for debugging the design and collecting data on the convergence of the DPD coefficient [48]. The design is targeted to a WARP v3 board is used. [49]. It features a Virtex 6 FPGA [50] and a Maxim Wi-Fi transceiver [30]. The board also uses the Anadigics AWL6951 dual-band power amplifier [51].

The WARP project provides an example template project for custom FPGA designs. The template includes all of the necessary modules for controlling the MAXIM transceiver, the ADC and DAC, the PA gain settings, clocks, etc. This is controlled with a microblaze core where C code can be used to set up the parameters and start the transmissions. In the main C code, we add the ability to communicate with a PC over UART to be able to send start, stop, and reset commands.

4.2   System Architecture

The architecture follows the algorithm closely. It is fully pipelined so that the training occurs rapidly in real-time. Each submodule for the design is discussed in detail in its corresponding subsection. In Figure 4.1, we show the top-level view of the design in the System Generator software.

4.2.1   Predistorter

The predistorter performs the work of the Equation 2.10. For the FPGA design, we are working with a memoryless DPD model and the third order IM3 distortion. With this, the previous eqation simplifies to become Equation 4.1

$$\tilde{x}(n) = x(n) + \alpha_{3+,3,0}\left(x_1(n)^2 x_2^*(n)\right) e^{j2\pi\frac{3f_{IF}}{f_s}n}. \tag{4.1}$$

In this equation, we need to compute the basis function, compute the complex sinusoid, perform a complex multiplication of the complex sinusoid and the basis function, and compute a complex multiplication of the shifted basis function and α.

It is required that the LTE transmitter provides the baseband component carriers to the module. The real and imaginary parts of each value are kept separate and each one is a 16.14, two's complement, fixed point value. The complex conjugate of
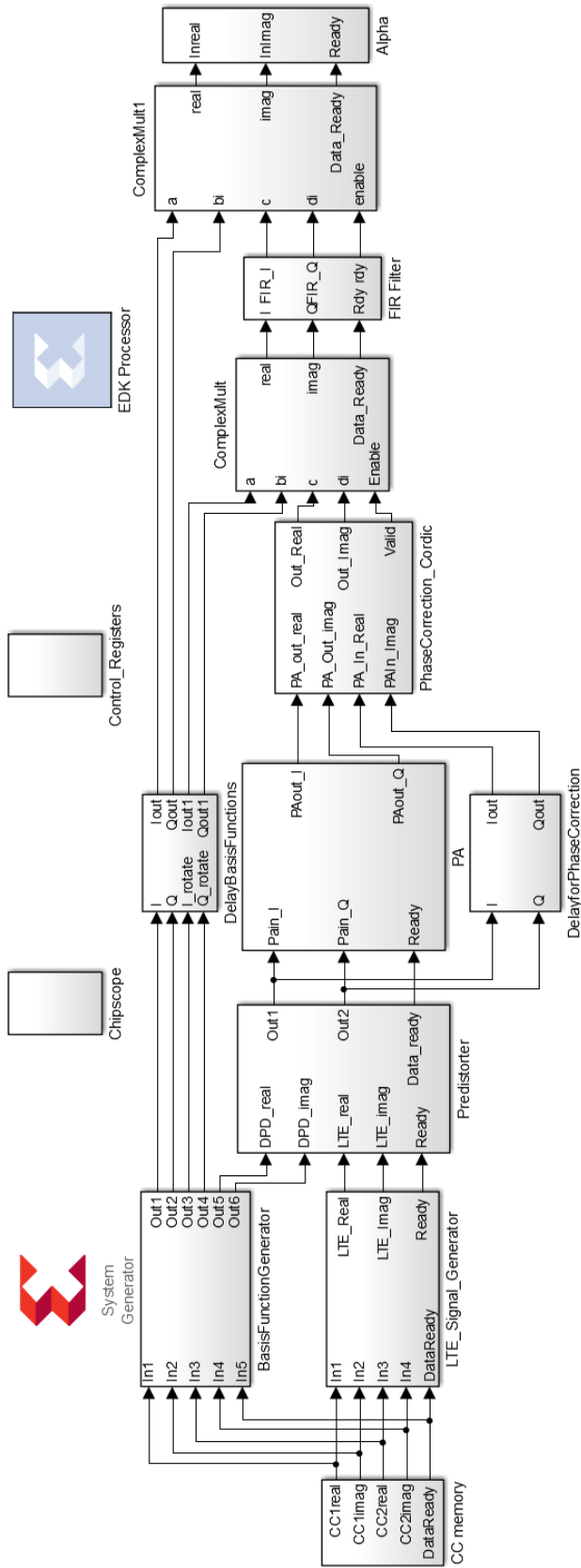
Figure 4.1: Top-level view of system generator design.

one of the basis functions is generated by simply a negation of the imaginary part of the data. The basis function is then generated by a series of complex multiplications. One of them is squared by multiplying it by itself. The result is then multiplied by the conjugate of the other component carrier. Appropriate pipeline registers are added so that data can stream through the design.

The frequency shift is done by a complex multiply. The complex sinusoid is precomputed and stored in a lookup table. Due to the cyclic nature of a sinusoid, the lookup table can be rotated through. The appropriate values are streamed into the complex multiply module where they are multiplied by the basis function. This result is then multiplied by α in another complex multiply. To complete the predistortion, this injection term is added to the LTE Signal. To make sure that the signals are combined properly, the LTE signal is delayed by the number of samples it takes to compute the injection signal. This PA input signal is written to the DAC so that transmission can start.

4.2.2   Time Synchronization

Values from the receiver ADC stream into the design after some time. This time delay is similar to what was discussed in Section 3.1.1. It is necessary to account for this. We assume that this is known and provide a register for this value to be stored. For our case, we use the value determined in the WARPLab environment which is usually 43 samples.

4.2.3   Phase Synchronization

As discussed in Section 3.1.1, there is also a constant phase shift between the transmitted signal and the received signal. It is necessary to correct for this. To do this, the PA input signal is delayed by the integer delay seen between the receiver and trans-

mitter that was stored in a register discussed in the previous paragraph. From there, the values stream into a coordinate rotation digital computer (CORDIC) module provided by Xilinx where the phase of the PA input and the PA output are computed. The difference between these two values is the phase shift. This phase shift is then streamed into another CORDIC module where the PA output is corrected by rotating the signal by the phase difference. We also implement a threshold to enable and disable the CORDIC phase estimation. Whenever the input or output magnitude is low, we hold whatever value we last had as a phase estimation. This prevents underflow errors that would cause an incorrect phase estimation. The CORDIC blocks are pipelined for continuous streaming through the design. This method allows for constant phase correction without any type of training before broadcasting.

4.2.4   Frequency Shift

The phase corrected PA output is then frequency shifted so that spur being suppressed is at baseband. This frequency shift is performed by a complex multiply of the PA output with a complex sinusoid. The complex sinusoid used earlier for adding the injection to the input signal is nearly identical. However, we need to shift in the opposite direction. To do this, we negate imaginary component and cycle through look-up-table similarly to earlier.

4.2.5   Feedback FIR Filter

A single FIR filter with two channels is used. The real and imaginary components are filtered independently with the same filter. To do this, a least-squares FIR filter was designed as discussed in Section 2.3. A 100 tap filter is used to adequately suppress the main carriers. The filter coefficients are statically set in the design. The filter is fully pipelined so that samples can stream through the design.

4.2.6   Training Module

The correlation is performed by correlating the filtered PA output with the appropriate basis function. For a memoryless single order correlation, this is effectively a single complex multiplication. The basis function that was computed for the predistortion submodule is fed forward to this with an appropriate delay to account for the power amplifier and the processing latency of the CORDIC block and FIR filter.

4.2.7   Block Length

This complex multiply is continuously computed during the learning block. The value computed is then constantly fed into an accumulator. The accumulator is enabled for the length of the learning block, L. This is controlled by a counter.

Assuming the block length is a power of 2, we divided our accumulator value by doing a right bit shift by the appropriate number of bits. We also assume that our LMS gain parameter μ is a power of 2. We combine the two into one single bit shift.

This value is sent to a subtractor that has the current value of α as the minuend and the suggested update to α as the subtrahend. The difference becomes the the new value of α. The subtraction is enabled only after the end of the learning block which is controlled by a counter. Because P was chosen as a power of two, we set the number of bits to be equal to the base 2 log of the block length.

Another counter controls the padding length. It is necessary that the padding length be at least as long as the loop delay through the system. We choose to set it to nearest power of 2 to facilitate easy implementation. The loop delay seen through the system is approximately 80 clock cycles. We choose L to have a length of 256 samples and M to be 128 samples. This choice in block lengths help to ensure stability and rapid convergence while choosing them to be powers of two helps with the computational complexity.

4.3 Experimental Setup

For the FPGA tests, we attach a WARPv3 board to an RF power splitter. One end goes to the RX port and the other goes to the spectrum analyzer. We do not have an LTE transmitter module. For that reason, we generate a signal offline and store it in the BRAM of the device. The signal stored in the BRAM is an LTE uplink signal with two 1.4 MHz carrier spaced 6 MHz apart.

The board is connected to a PC via UART over the micro USB cable. The design includes commands such as start, stop, reset, and delay parameters that can be controlled over UART. The onboard C code in the microblaze writes to registers that the hardware design then uses. A Xilinx JTAG connector also connect the WARP board to the PC. This is used mostly for debugging purposes, but is also used to collect data on the convergence of the DPD coefficient α.

4.4 Results

In Figure 4.3, we see the results for suppression of the IM3+ spur using the real-time implementation on the FPGA. Here we see 12 dB of suppression. Note that this result was obtained from a different board then most of the other results presented in this thesis. Amounts of suppression, as shown earlier, can vary between boards. This result is plotted using data from a spectrum analyzer.

In Figure 4.3, we see the convergence of the coefficients. Here the basis functions are not normalized, hence the magnitude is much different than previous WARPLab results. However, we see rapid convergence and relative stability for the coefficient.
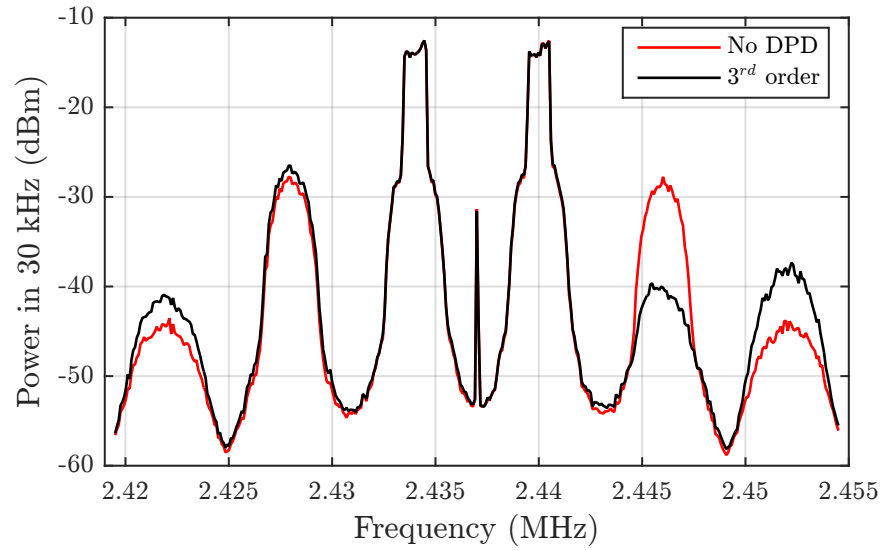
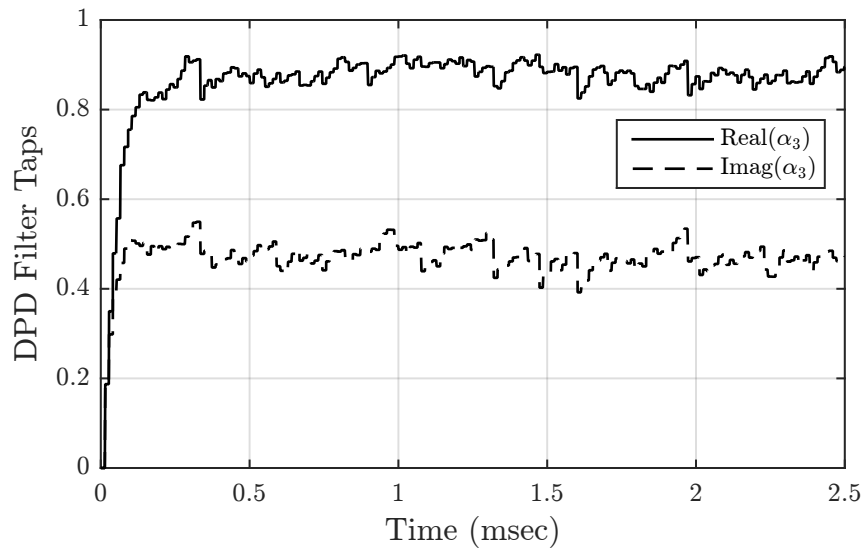Figure 4.2: Spectrum with and without DPD using the FPGA for processing

Figure 4.3: Convergence of DPD coefficients for FPGA implementation

4.4.1 Utilization

Most of the multiplications in the architecture are done in specialized hardware multiplier units of the Virtex 6 known as DSP48E1 slices. When generated, the DPD module uses a total of 242 DSP48E1 slices out of the 768 available DSP48E1 slices. Of this, many are being used by an order 100 FIR filter to extract a block of the IM3 spurious emission error samples. Currently the FPGA design focuses on performance. For better performance/utilization tradeoff, the number of DSP48E1 slices could be significantly reduced with further optimization.

4.4.2 Timing

The module runs at the same clock frequency as the ADC and DAC of the WARP board which is 40 MHz. The maximum possible clock rate for the design is 103 MHz. Once the DPD coefficient α converges, the module introduces a small latency of 13 additional clock cycles for passing the LTE signal from BRAM to PA. This latency accounts for the digital predistortion injection using the estimated DPD coefficient. This low overhead for implementation shows the feasibility of the sub-band DPD for real mobile systems.

CONCLUSIONS

In this thesis, we have evaluated a sub-band, digital predistortion algorithm for performance and feasibility on real hardware. We have shown through WARPLab that up to ninth-order power amplifier nonlinearities can be corrected reliably for a variety of different scenarios. Moreover, we show that the algorithm is feasible for a real-time FPGA implementation. Overall, we have shown that it is possible to suppress undesired intermodulation distortion spurious emissions by over 20 dB. This work is novel in that it is done using a real power amplifier as opposed to being entirely simulation based.

5.1 Future Work

This work has opened of many possibilities for continued research. In WARPLab, we would like to further investigate larger carriers and more carriers. As stated in the introduction, the LTE standard allows for up to five carriers and there are currently devices that allow for up to three. In this thesis, we have considered only up to two carriers. To be more compliant with the technology and standards, we must account for the possibility of more carriers.

Moreover, to be more compliant with standards, we will further consider how this work may fit in to the LTE frame structure. The training shown in the majority of the plots took approximately 10 ms. This corresponds with an entire frame [52]. An entire frame may be too much overhead for training especially when considering how quickly the user may be reassigned to new channels. The DPD from this thesis will further be studied in this context in future work.

Moreover, we will consider how often the basestation reassigns a mobile user to a new channel configuration. For scenarios where the user is reassigned more often, the training overhead for each new scenario is not feasible. We will consider the possibility of storing old coefficients to facilitate more rapid training.

We would also like to continue FPGA development to implement DPD that accounts for higher order PA nonlinearities. Using the orthogonalization methods presented in this thesis, we will be able to train higher order distortions by simply swapping out basis functions in the current design. This would allow us to serially train coefficients until we get the necessary suppression. This sort of method allows for additional performance with minimal additional hardware. In the spirit of Figure 3.23, it is also possible to use the same hardware to train multiple spurs. This is another area for further development.

We would also consider building a custom PCB for broadcasting that includes a separate upconverter for the predistortion signal. Currently, the injected DPD signal must be in the TX window which is determined by sample rates of the ADC/DAC. This limits the carrier bandwidths and spacings that we can predistort the IM3 on WARP. By transmitting the injection independently, we would be able to handle any arbitrary carrier spacing.

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